

PCB STACK UP

LAYER 1 : TOP
LAYER 2 : SGND1
LAYER 3 : IN1
LAYER 4 : IN2
LAYER 5 : VCC
LAYER 6 : IN3
LAYER 7 : SGND2
LAYER 8 : BOT

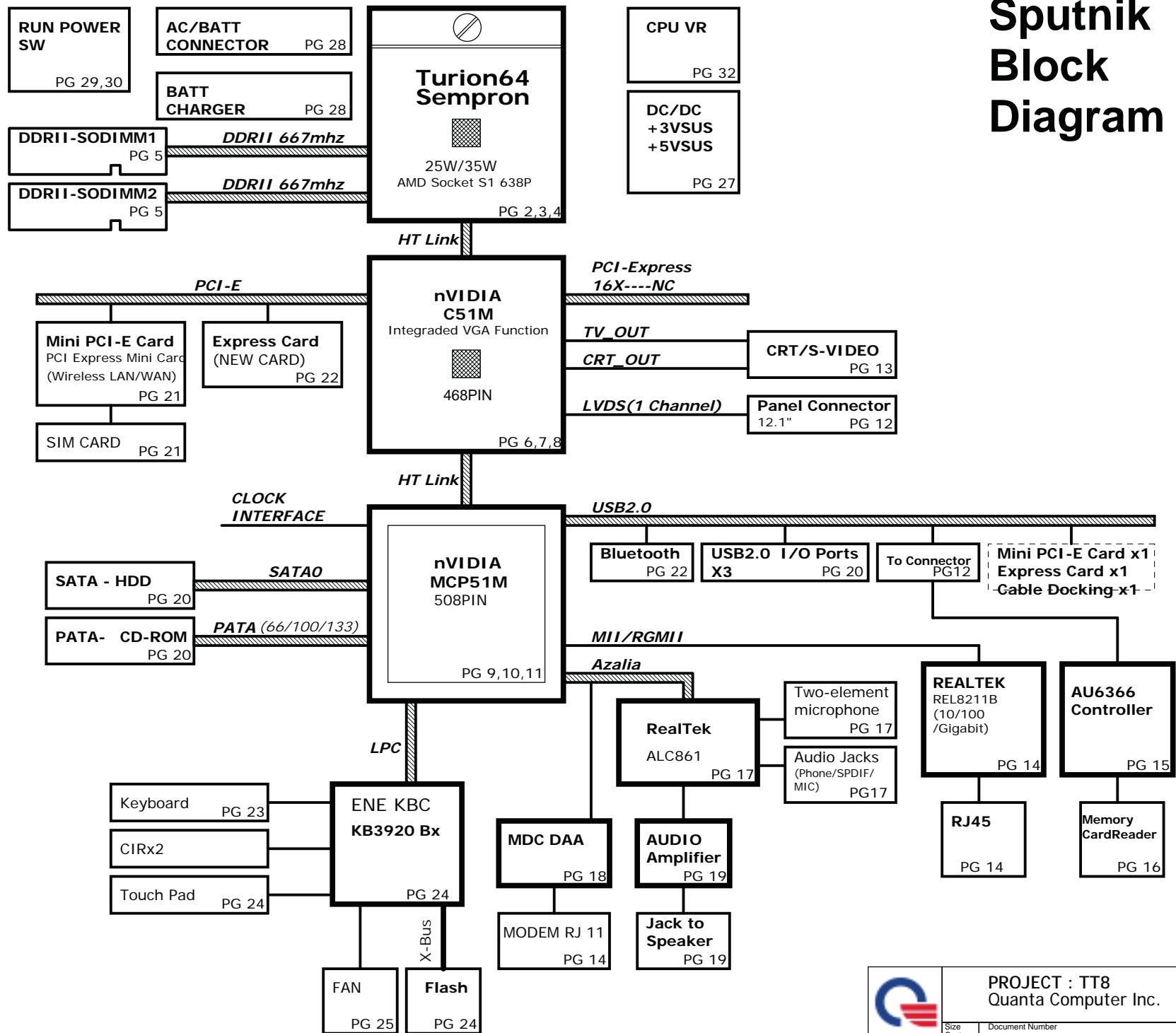
Cable Docking

TV_OUT
VGA
RJ-45
CIR/Pwr btn
SPDIF Out
Stereo MIC
Headphone Jack
USB Port
VOL Cntr

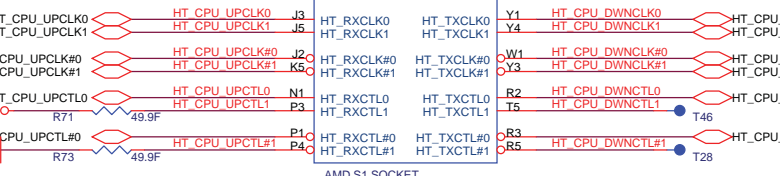
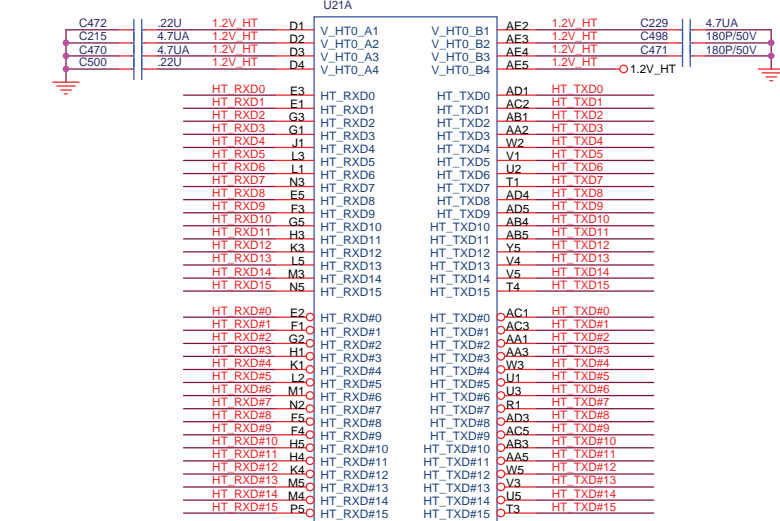
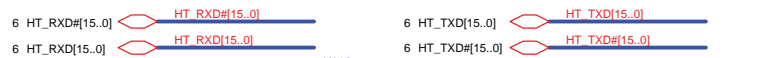
PG 25

VAULE DEFINE
A=0603,B=0805,C=1206,F=1%,
OTHER IS 0402

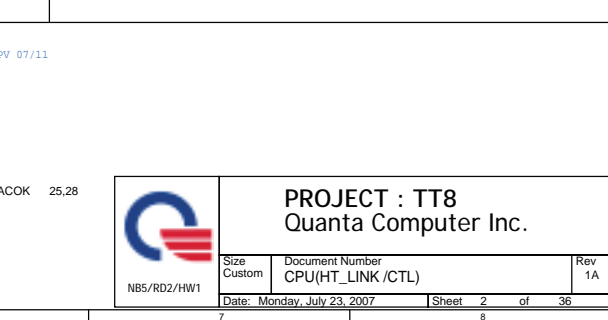
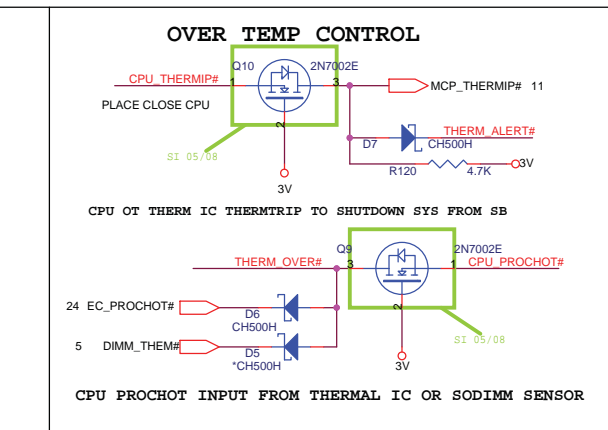
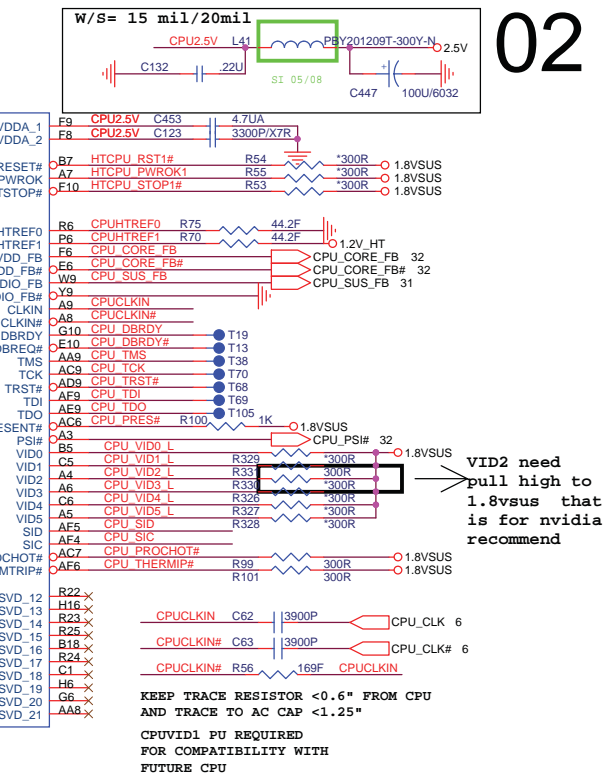
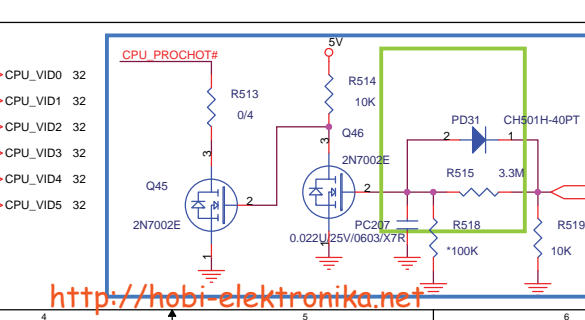
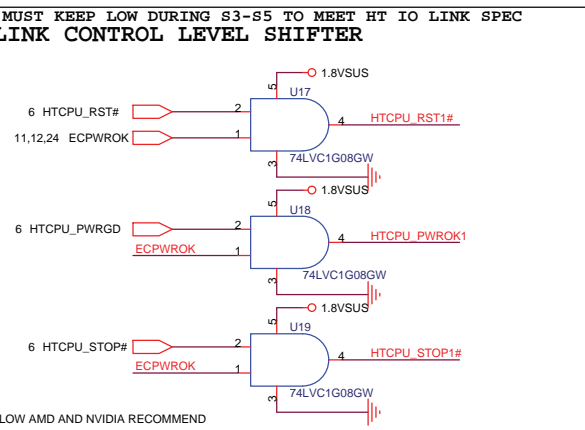
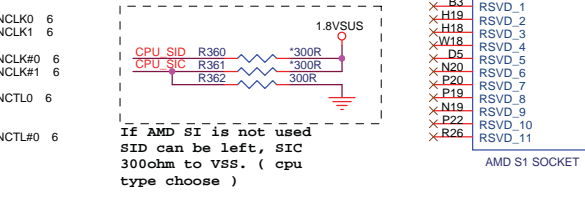
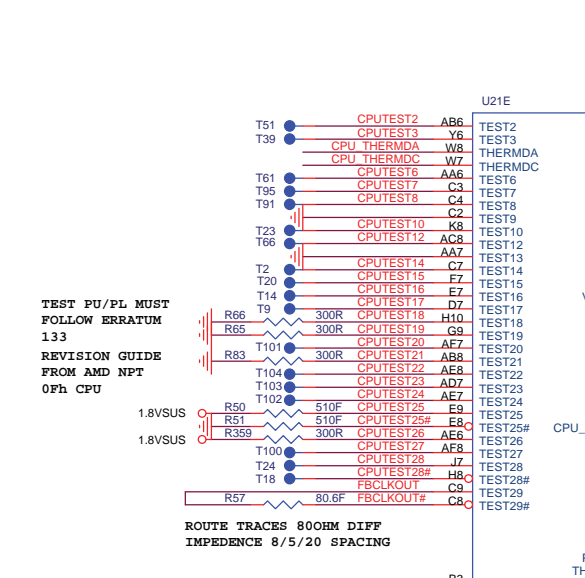
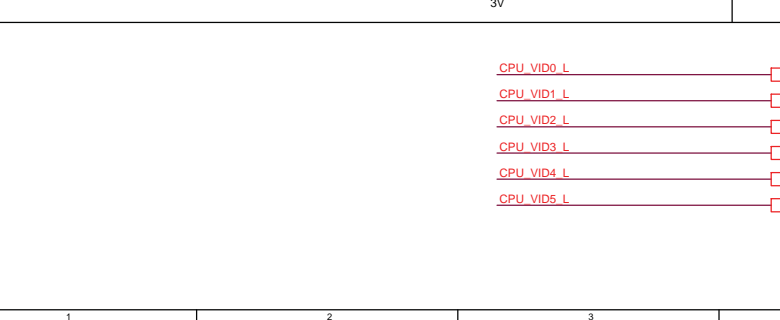
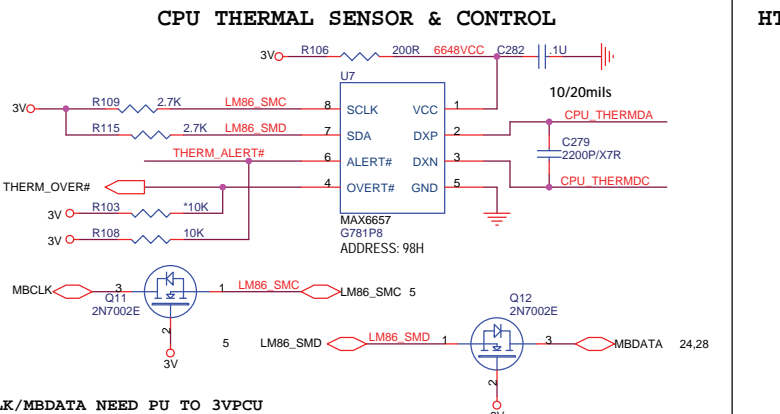
EXAMPLE
10R=10ohm(0402)
10A=10ohm(0603)
10B=10ohm(0805)
10C=10ohm(1206)
10/F=10ohm(0402 and 1%)



Sputnik Block Diagram



HT_RXCTL1/HT_RXCTL#1 MUST <1.5" FROM CPU PIN



U21B

M A DQ63 AA12	MA_DATA[63]	MA_DM[7]	Y13 M A DQM7
M A DQ62 AB12	MA_DATA[62]	MA_DM[6]	AB16 M A DQM6
M A DQ61 AA14	MA_DATA[61]	MA_DM[5]	Y19 M A DQM5
M A DQ60 AB14	MA_DATA[60]	MA_DM[4]	AC24 M A DQM4
M A DQ59 W11	MA_DATA[59]	MA_DM[3]	E24 M A DQM3
M A DQ58 Y12	MA_DATA[58]	MA_DM[2]	E19 M A DQM2
M A DQ57 AD13	MA_DATA[57]	MA_DM[1]	C15 M A DQM1
M A DQ56 AB13	MA_DATA[56]	MA_DM[0]	E12 M A DQM0
M A DQ55 AD15	MA_DATA[55]		
M A DQ54 AB15	MA_DATA[54]		
M A DQ53 AB17	MA_DATA[53]		
M A DQ52 Y17	MA_DATA[52]	MA_DQS[7]	W12 M A DQS7
M A DQ51 Y14	MA_DATA[51]	MA_DQS[6]	Y15 M A DQS6
M A DQ50 W14	MA_DATA[50]	MA_DQS[5]	AB19 M A DQS5
M A DQ49 W16	MA_DATA[49]	MA_DQS[4]	AD23 M A DQS4
M A DQ48 AD17	MA_DATA[48]	MA_DQS[3]	G22 M A DQS3
M A DQ47 Y18	MA_DATA[47]	MA_DQS[2]	C22 M A DQS2
M A DQ46 AD19	MA_DATA[46]	MA_DQS[1]	G16 M A DQS1
M A DQ45 AD21	MA_DATA[45]	MA_DQS[0]	G13 M A DQS0
M A DQ44 AB21	MA_DATA[44]	MA_DQS[7]	W13 M A DQS7
M A DQ43 AB18	MA_DATA[43]	MA_DQS[6]	W15 M A DQS6
M A DQ42 AA18	MA_DATA[42]	MA_DQS[5]	AB20 M A DQS5
M A DQ41 AA20	MA_DATA[41]	MA_DQS[4]	AC23 M A DQS4
M A DQ40 Y20	MA_DATA[40]	MA_DQS[3]	G21 M A DQS3
M A DQ39 AA22	MA_DATA[39]	MA_DQS[2]	C21 M A DQS2
M A DQ38 Y22	MA_DATA[38]	MA_DQS[1]	G15 M A DQS1
M A DQ37 W21	MA_DATA[37]	MA_DQS[0]	H13 M A DQS0
M A DQ36 W22	MA_DATA[36]		
M A DQ35 AA21	MA_DATA[35]		
M A DQ34 AB22	MA_DATA[34]		
M A DQ33 AB24	MA_DATA[33]		
M A DQ32 Y24	MA_DATA[32]		
M A DQ31 H22	MA_DATA[31]		
M A DQ30 H20	MA_DATA[30]		
M A DQ29 E22	MA_DATA[29]		
M A DQ28 E21	MA_DATA[28]		
M A DQ27 J19	MA_DATA[27]		
M A DQ26 F22	MA_DATA[26]		
M A DQ25 F22	MA_DATA[25]		
M A DQ24 F20	MA_DATA[24]		
M A DQ23 C23	MA_DATA[23]		
M A DQ22 B22	MA_DATA[22]		
M A DQ21 F18	MA_DATA[21]		
M A DQ20 E16	MA_DATA[20]		
M A DQ19 E20	MA_DATA[19]		
M A DQ18 D22	MA_DATA[18]		
M A DQ17 C19	MA_DATA[17]		
M A DQ16 G18	MA_DATA[16]		
M A DQ15 G17	MA_DATA[15]		
M A DQ14 C17	MA_DATA[14]		
M A DQ13 E14	MA_DATA[13]		
M A DQ12 E14	MA_DATA[12]		
M A DQ11 H17	MA_DATA[11]		
M A DQ10 E17	MA_DATA[10]		
M A DQ9 E15	MA_DATA[9]		
M A DQ8 H15	MA_DATA[8]		
M A DQ7 E13	MA_DATA[7]		
M A DQ6 C13	MA_DATA[6]		
M A DQ5 H12	MA_DATA[5]		
M A DQ4 H11	MA_DATA[4]		
M A DQ3 G14	MA_DATA[3]		
M A DQ2 H14	MA_DATA[2]		
M A DQ1 F12	MA_DATA[1]		
M A DQ0 G12	MA_DATA[0]		

AMD S1 SOCKET

M A DQ[63..0]	M A DQM[7..0]	M A DQM[7..0] 5
M A DQS[7..0]	M A DQS[7..0] 5	M A DQS[7..0] 5
M A BA[2..0]	M A BA[2..0] 4,5	M A BA[2..0] 4,5
M A CS[3..0]	M A CS[3..0] 4,5	M A CS[3..0] 4,5
M A RAS#	M A RAS# 4,5	M A RAS# 4,5
M A CAS#	M A CAS# 4,5	M A CAS# 4,5
M A WE#	M A WE# 4,5	M A WE# 4,5
M A CKE1	M A CKE1 4,5	M A CKE1 4,5
M A CKE0	M A CKE0 4,5	M A CKE0 4,5
M A ODT1	M A ODT1 4,5	M A ODT1 4,5
M A ODT0	M A ODT0 4,5	M A ODT0 4,5

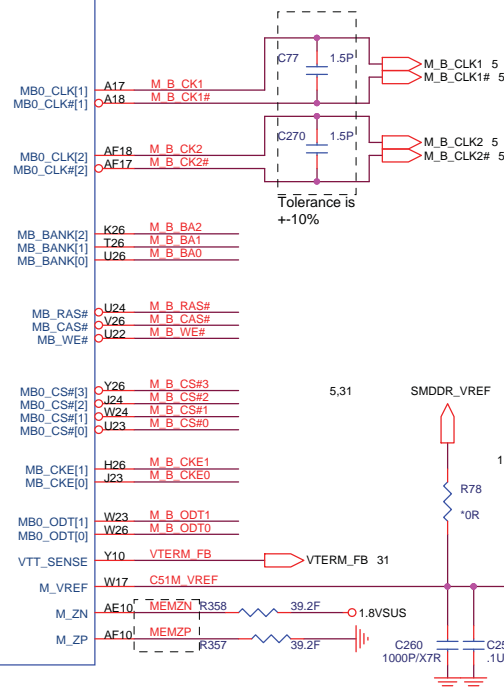
U21C

M B DQ63 AD11	MB_DATA[63]	MB_DM[7]	AD12 M B DQM7
M B DQ62 AF11	MB_DATA[62]	MB_DM[6]	AC16 M B DQM6
M B DQ61 AF14	MB_DATA[61]	MB_DM[5]	AE22 M B DQM5
M B DQ60 Y14	MB_DATA[60]	MB_DM[4]	E25 M B DQM4
M B DQ59 Y14	MB_DATA[59]	MB_DM[3]	E25 M B DQM3
M B DQ58 AB11	MB_DATA[58]	MB_DM[2]	A22 M B DQM2
M B DQ57 AC12	MB_DATA[57]	MB_DM[1]	B16 M B DQM1
M B DQ56 AF13	MB_DATA[56]	MB_DM[0]	A12 M B DQM0
M B DQ55 AF15	MB_DATA[55]		
M B DQ54 AF16	MB_DATA[54]		
M B DQ53 AC18	MB_DATA[53]		
M B DQ52 AF19	MB_DATA[52]	MB_DQS[7]	AF12 M B DQS7
M B DQ51 AD14	MB_DATA[51]	MB_DQS[6]	AE16 M B DQS6
M B DQ50 AC14	MB_DATA[50]	MB_DQS[5]	AF21 M B DQS5
M B DQ49 Y14	MB_DATA[49]	MB_DQS[4]	AC25 M B DQS4
M B DQ48 AC18	MB_DATA[48]	MB_DQS[3]	F26 M B DQS3
M B DQ47 AD20	MB_DATA[47]	MB_DQS[2]	A24 M B DQS2
M B DQ46 AC20	MB_DATA[46]	MB_DQS[1]	D16 M B DQS1
M B DQ45 AF23	MB_DATA[45]	MB_DQS[0]	C12 M B DQS0
M B DQ44 AF24	MB_DATA[44]	MB_DQS[7]	AE12 M B DQS7
M B DQ43 AC20	MB_DATA[43]	MB_DQS[6]	AD16 M B DQS6
M B DQ42 AF20	MB_DATA[42]	MB_DQS[5]	AF22 M B DQS5
M B DQ41 AD22	MB_DATA[41]	MB_DQS[4]	AC26 M B DQS4
M B DQ40 AC22	MB_DATA[40]	MB_DQS[3]	E26 M B DQS3
M B DQ39 AE25	MB_DATA[39]	MB_DQS[2]	A23 M B DQS2
M B DQ38 AD26	MB_DATA[38]	MB_DQS[1]	C16 M B DQS1
M B DQ37 AA25	MB_DATA[37]	MB_DQS[0]	B12 M B DQS0
M B DQ36 AA25	MB_DATA[36]		
M B DQ35 AE24	MB_DATA[35]		
M B DQ34 AD24	MB_DATA[34]		
M B DQ33 AA23	MB_DATA[33]		
M B DQ32 G24	MB_DATA[32]		
M B DQ31 G24	MB_DATA[31]		
M B DQ30 G23	MB_DATA[30]		
M B DQ29 D26	MB_DATA[29]		
M B DQ28 C26	MB_DATA[28]		
M B DQ27 G26	MB_DATA[27]		
M B DQ26 G25	MB_DATA[26]		
M B DQ25 E24	MB_DATA[25]		
M B DQ24 E23	MB_DATA[24]		
M B DQ23 C24	MB_DATA[23]		
M B DQ22 B24	MB_DATA[22]		
M B DQ21 C20	MB_DATA[21]		
M B DQ20 B20	MB_DATA[20]		
M B DQ19 C25	MB_DATA[19]		
M B DQ18 D24	MB_DATA[18]		
M B DQ17 A21	MB_DATA[17]		
M B DQ16 D20	MB_DATA[16]		
M B DQ15 D18	MB_DATA[15]		
M B DQ14 C18	MB_DATA[14]		
M B DQ13 D14	MB_DATA[13]		
M B DQ12 C14	MB_DATA[12]		
M B DQ11 A20	MB_DATA[11]		
M B DQ10 A19	MB_DATA[10]		
M B DQ9 A16	MB_DATA[9]		
M B DQ8 A15	MB_DATA[8]		
M B DQ7 A13	MB_DATA[7]		
M B DQ6 D12	MB_DATA[6]		
M B DQ5 E11	MB_DATA[5]		
M B DQ4 G11	MB_DATA[4]		
M B DQ3 B14	MB_DATA[3]		
M B DQ2 A14	MB_DATA[2]		
M B DQ1 A11	MB_DATA[1]		
M B DQ0 C11	MB_DATA[0]		

AMD S1 SOCKET

5 M B DQ[63..0]	M B DQ[63..0]	M B DQ[63..0] 5
4,5 M B A[15..0]	M B A[15..0]	M B A[15..0] 5

M B DQM[7..0]	M B DQM[7..0] 5	M B DQM[7..0] 5
M B DQS[7..0]	M B DQS[7..0] 5	M B DQS[7..0] 5
M B BA[2..0]	M B BA[2..0] 4,5	M B BA[2..0] 4,5
M B CS[3..0]	M B CS[3..0] 4,5	M B CS[3..0] 4,5
M B RAS#	M B RAS# 4,5	M B RAS# 4,5
M B CAS#	M B CAS# 4,5	M B CAS# 4,5
M B WE#	M B WE# 4,5	M B WE# 4,5
M B CKE1	M B CKE1 4,5	M B CKE1 4,5
M B CKE0	M B CKE0 4,5	M B CKE0 4,5
M B ODT1	M B ODT1 4,5	M B ODT1 4,5
M B ODT0	M B ODT0 4,5	M B ODT0 4,5

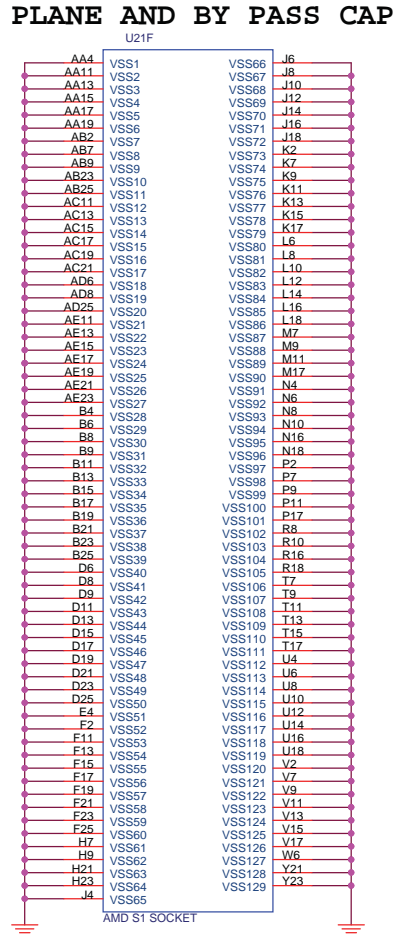
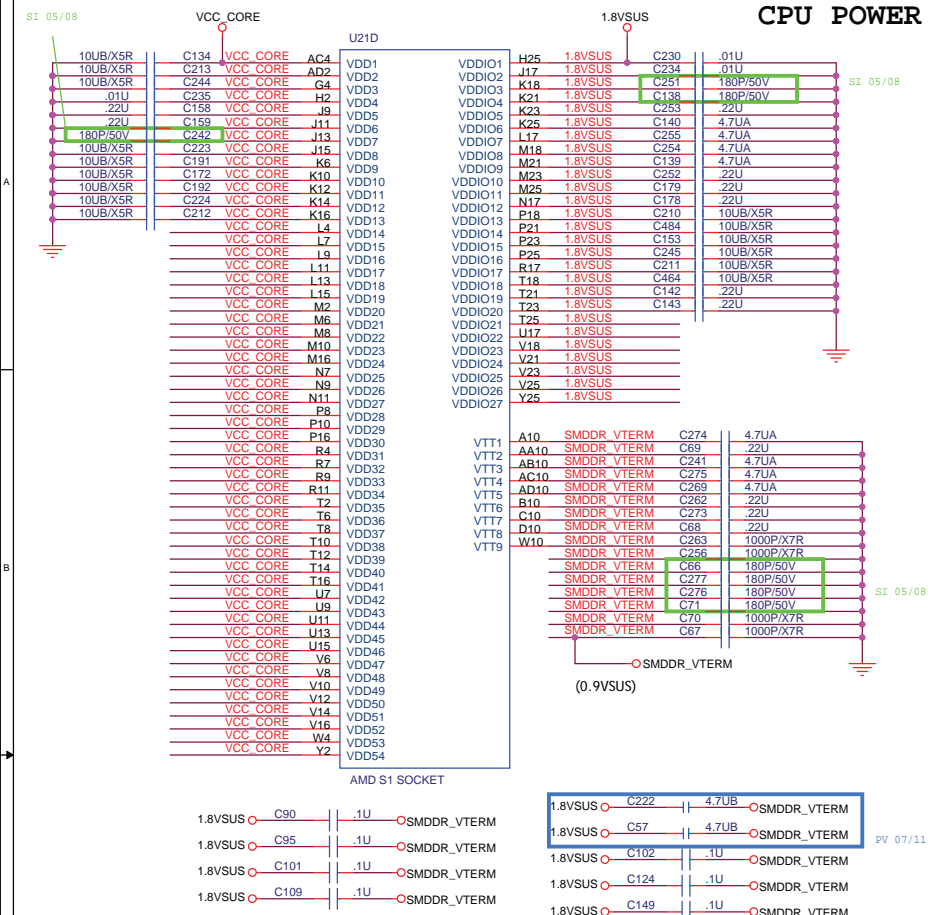
TRACE FROM CAP TO CPU MUST BE LESS
THAN 1200MILS MAX NECKDOWN TO &
FROM CAPS IS 500MILS

C51MVREF : W =20MIL AND SPACE = 20MIL

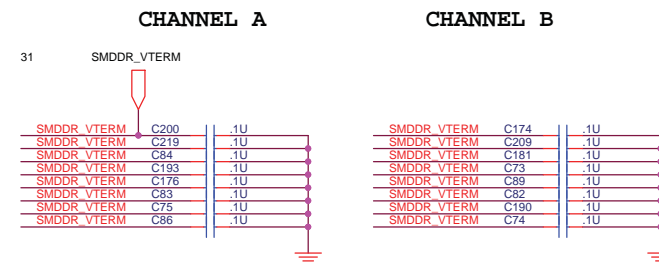
PROJECT : TT8
Quanta Computer Inc.

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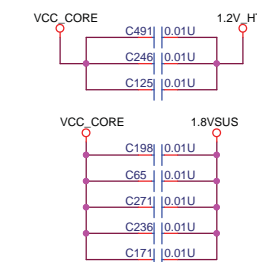
CPU POWER PLANE AND BY PASS CAP



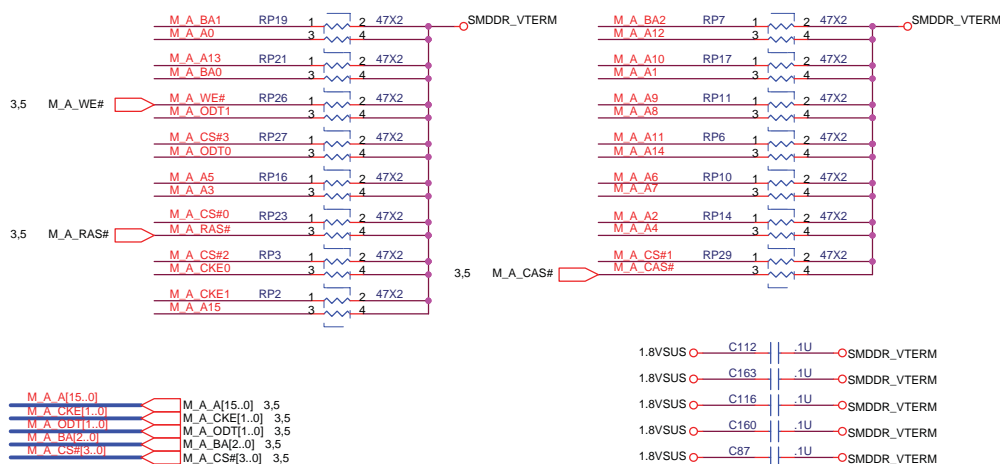
DDR2 TERMINATION BYPASS CAP



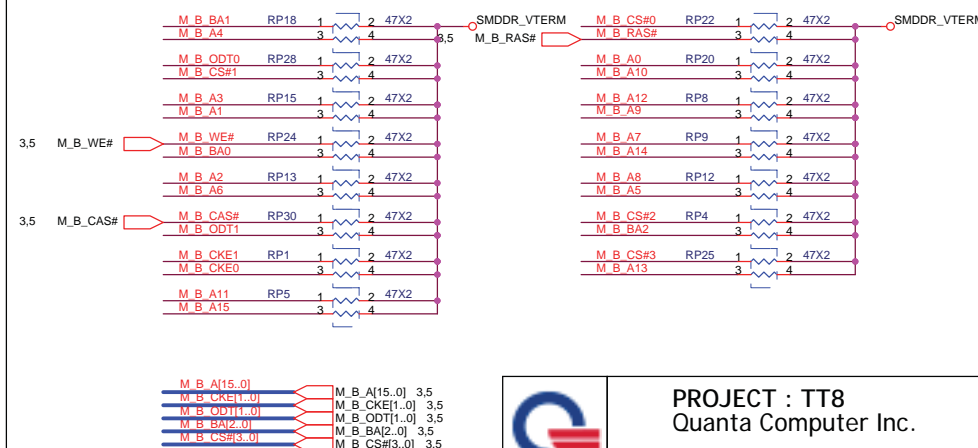
Layout note: Place one cap close to every 2
pullup resistors terminated to
SMDDR VTERM

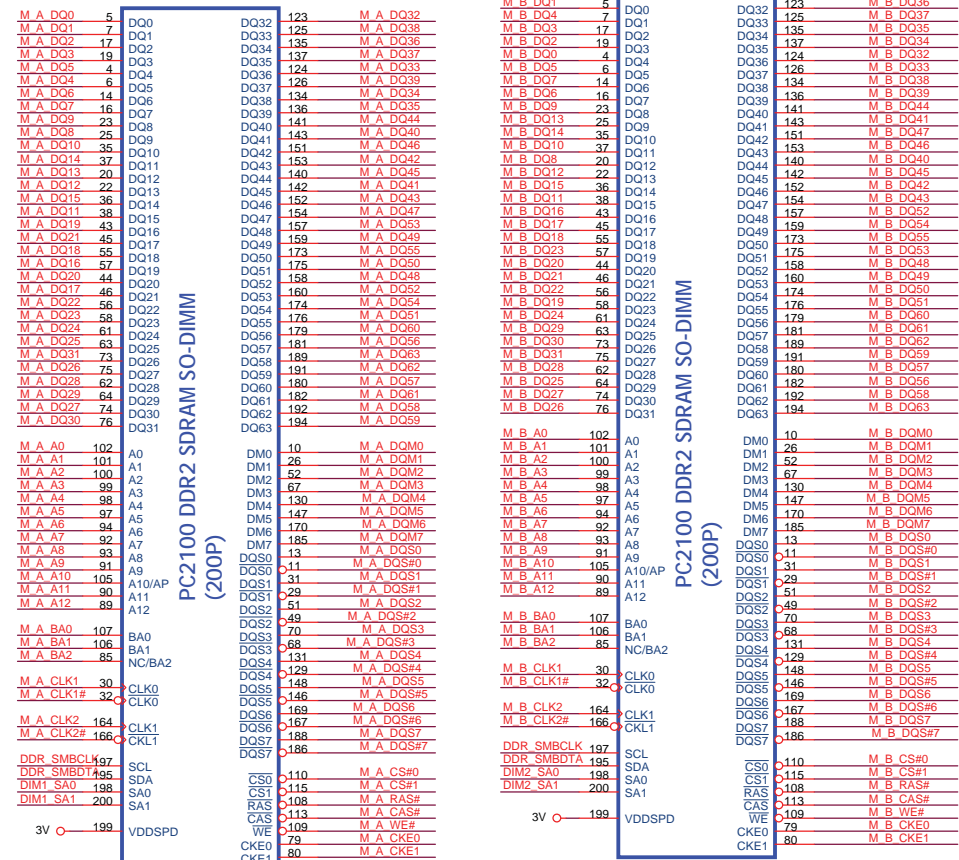
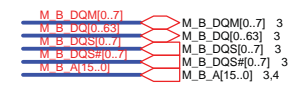
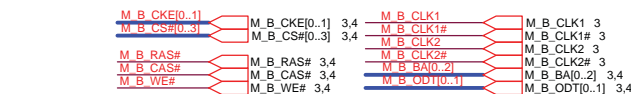
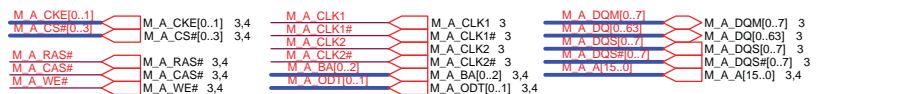


DDRII CHANNEL A TERMINATION



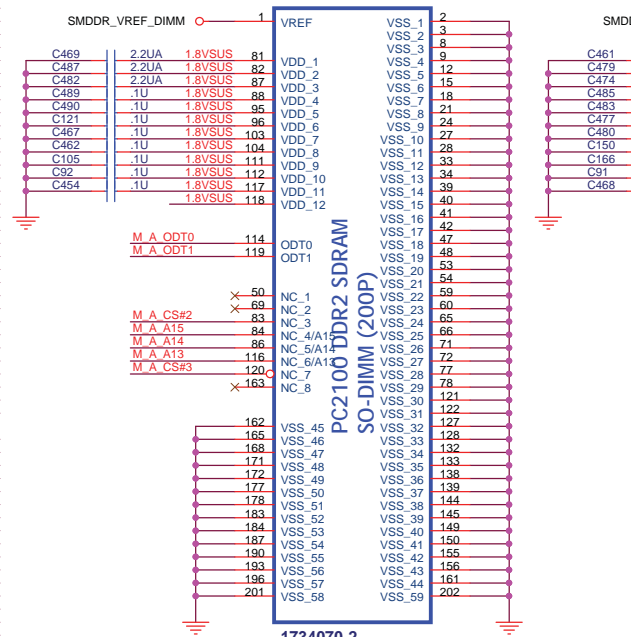
DDRII CHANNEL B TERMINATION





CKE 0,1
REV type : H 6.5

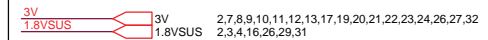
CKE 2,3
REV type : H 11



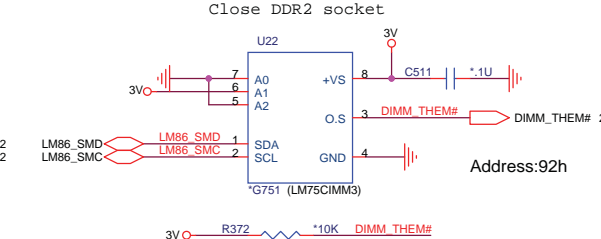
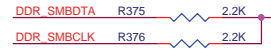
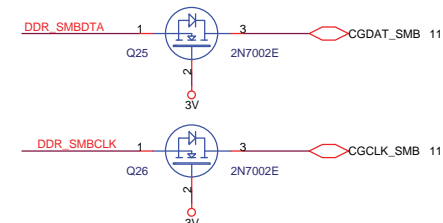
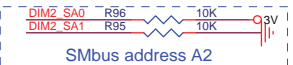
SO-DIMM BYPASS PLACEMENT :

Place these Caps near So-Dimm1.

No Vias Between the Trace of PIN to CAP.



SMDDR_VREF_DIMM :
TRACE WIDTH > 20 MIL
PUT BYPASS CAP ON EACH DIMM

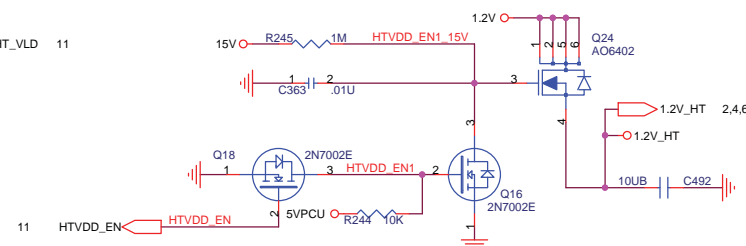
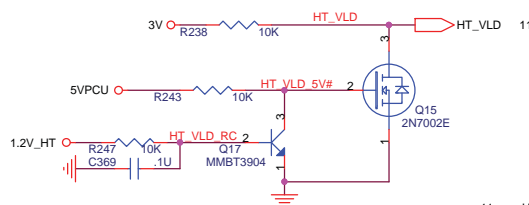
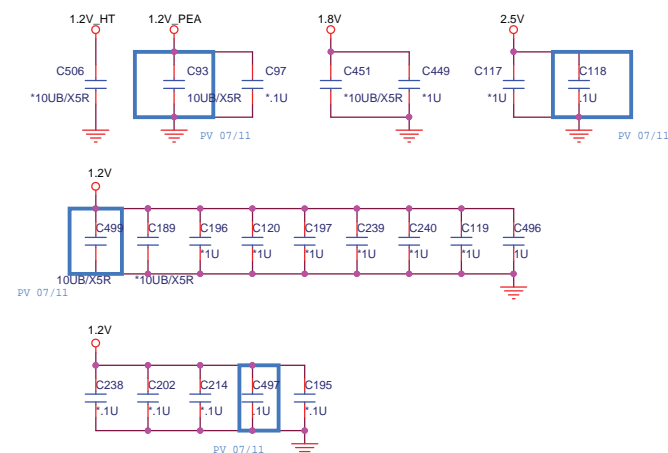
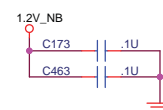
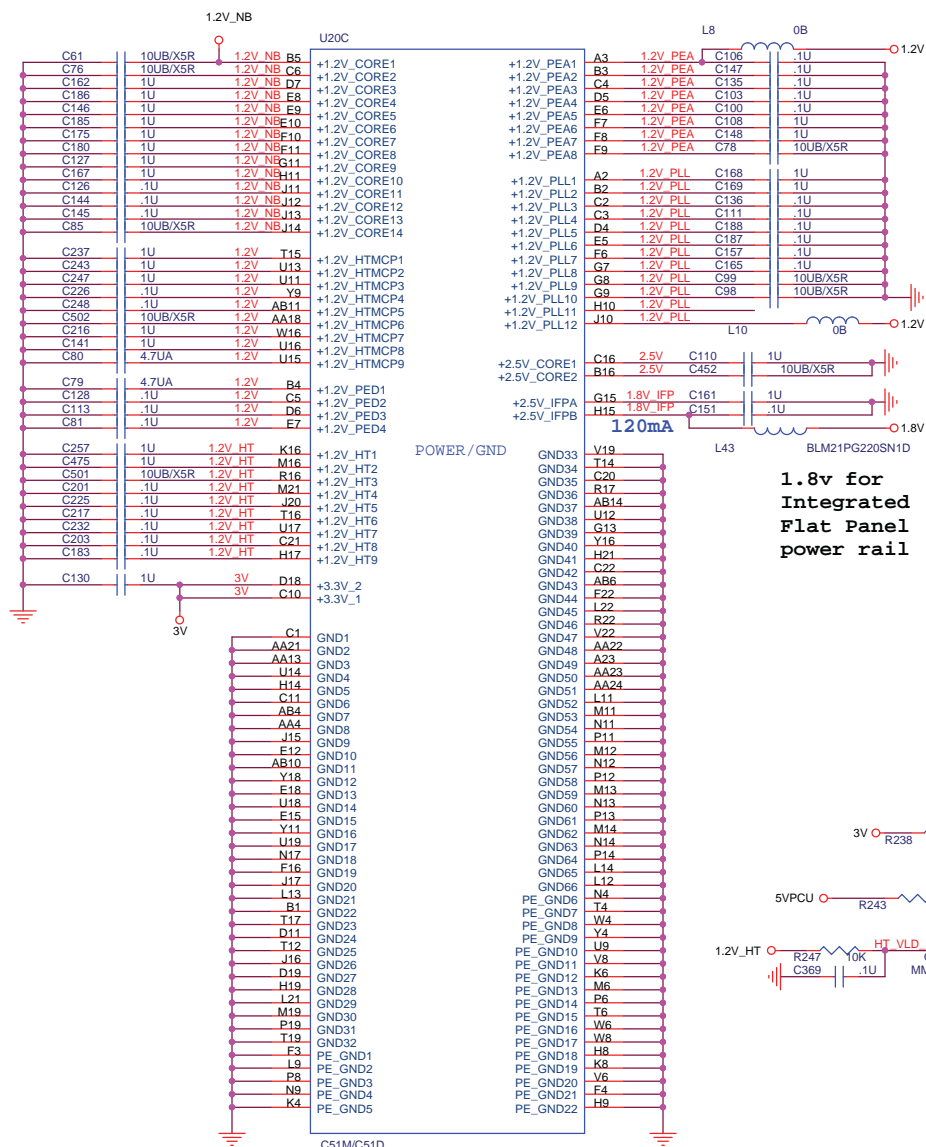


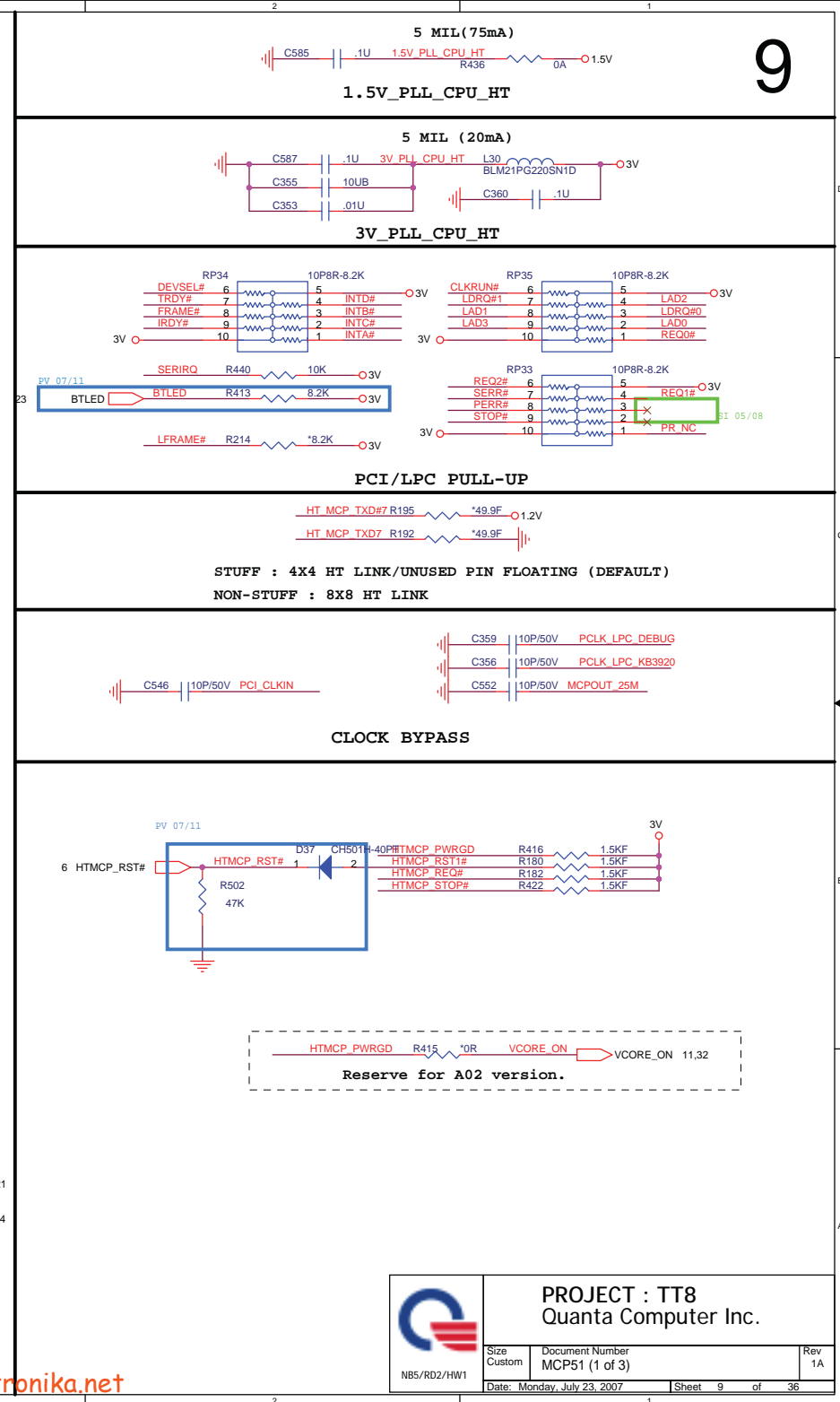
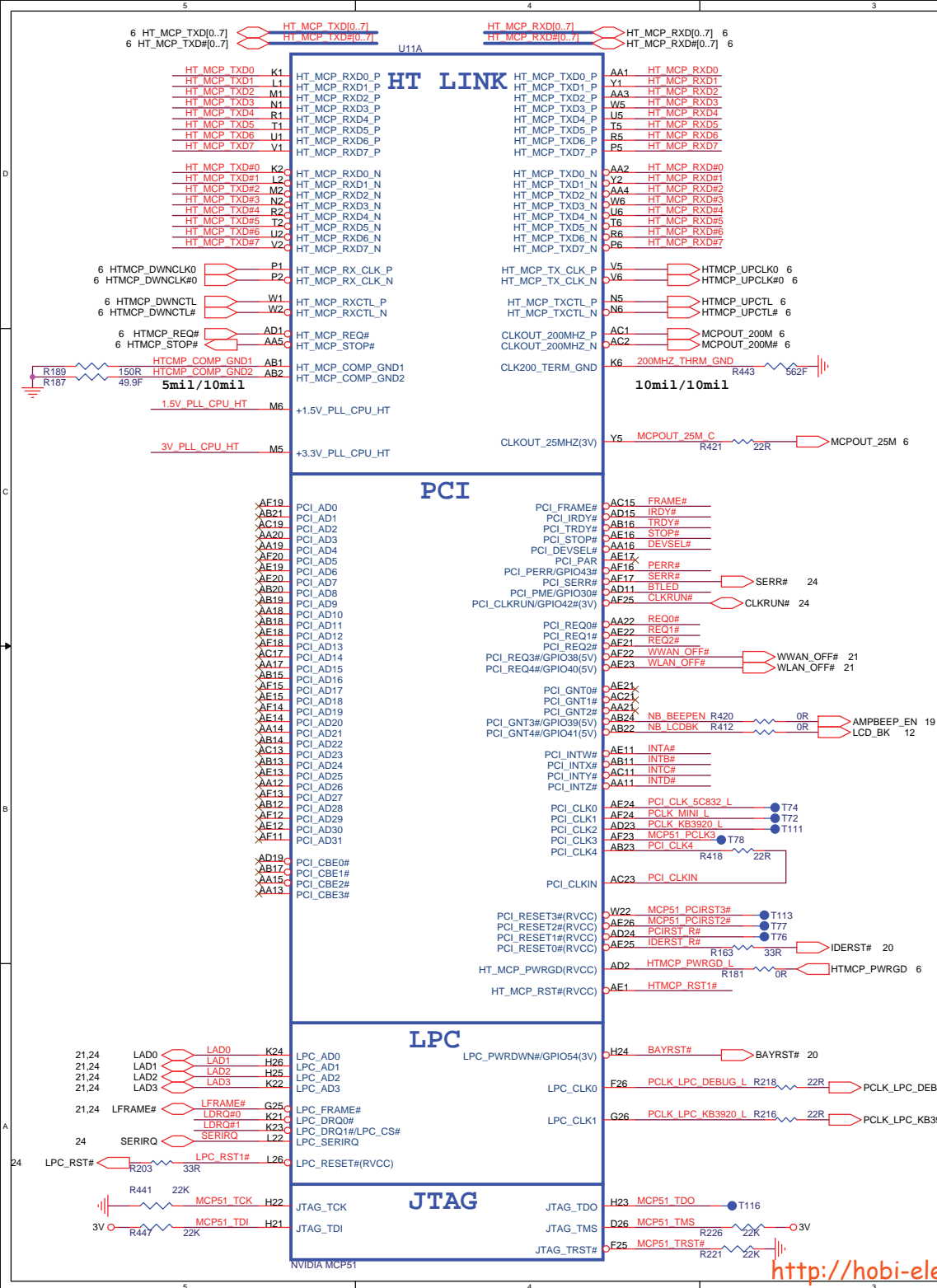
PROJECT : TT8
Quanta Computer Inc.

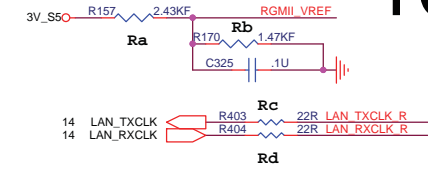
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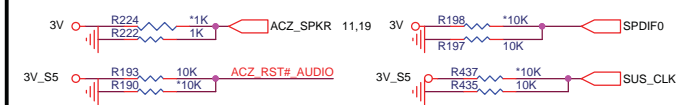
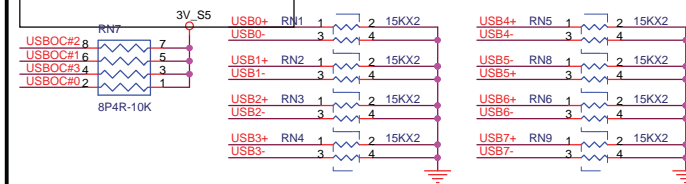
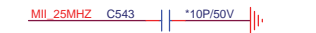
C51M POWER PLANE/GND & BYPASS







	10/100	GIGA
VREF	1.65V	1.25V
Ra	1K/F	2.43K/F
Rb	1K/F	1.47K/F
Rc	0R	22R
Rd	0R	22R
Re	NC	0R
Rf	NC	0R
Rg	NC	0R



ACZ SPKR STRAP (Boot MODE)	
0	User Table*
1	Safe table

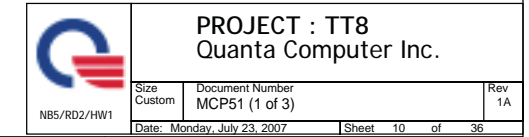
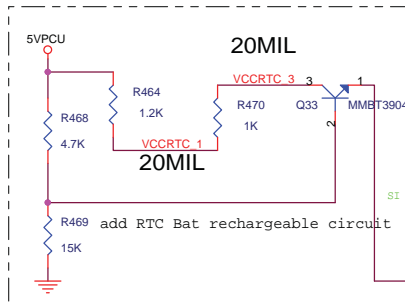
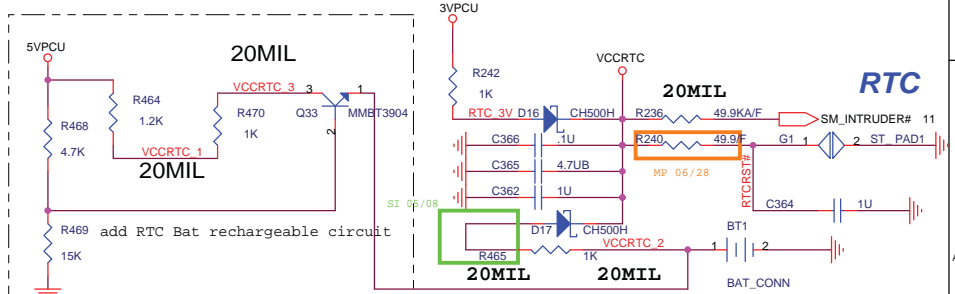
ACZ RST# STRAP (LAN)	
0	MII
1	RGMII*

*DEFAULT

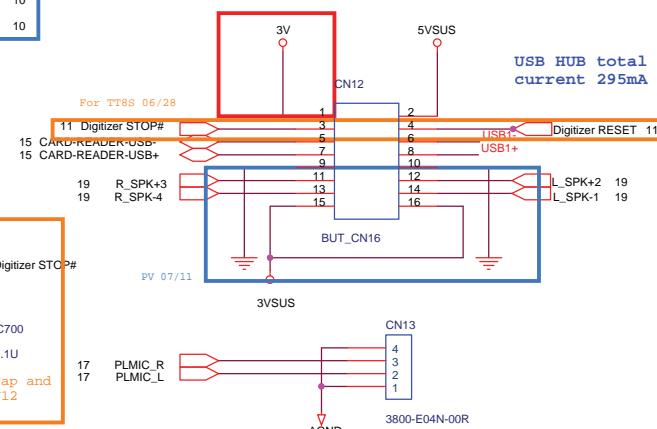
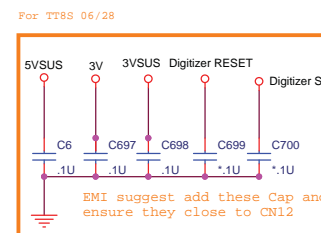
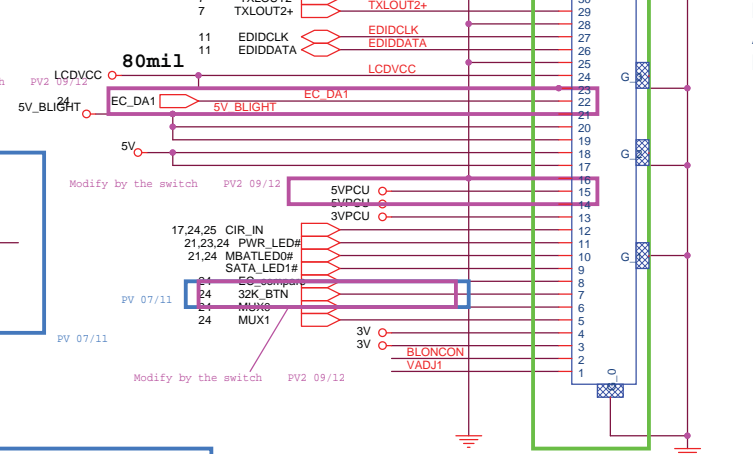
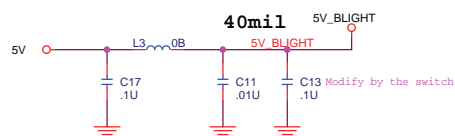
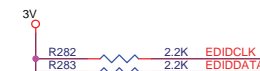
SPDIF0 STRAP (SIO CLK)	
0	14.318MHZ*
1	24.000MHZ

SUSCLK STRAP (MCP MODE)	
0	NORMAL*
1	SLAVE

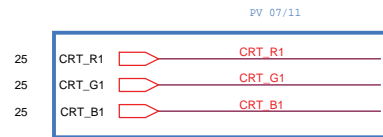
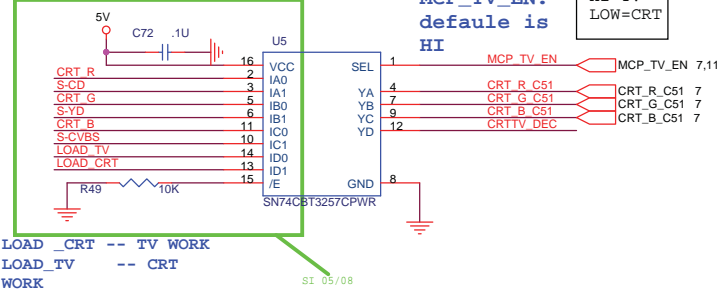
*DEFAULT



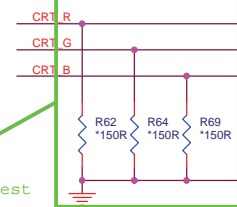




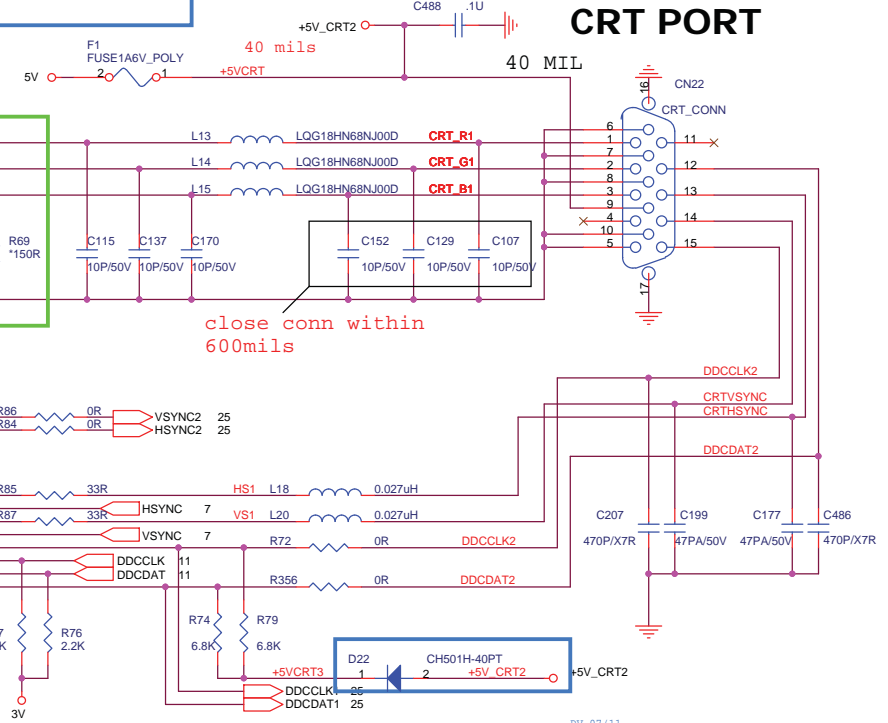
CRT/TV SWITCH



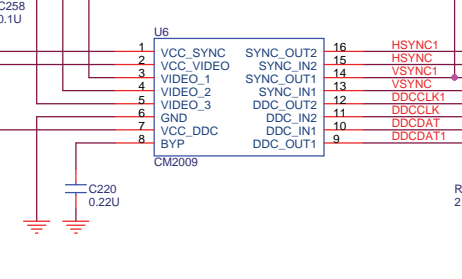
150-R as possible as closed to CRT connector (close with in 600 mil)



CRT PORT



ESD PROTECTION

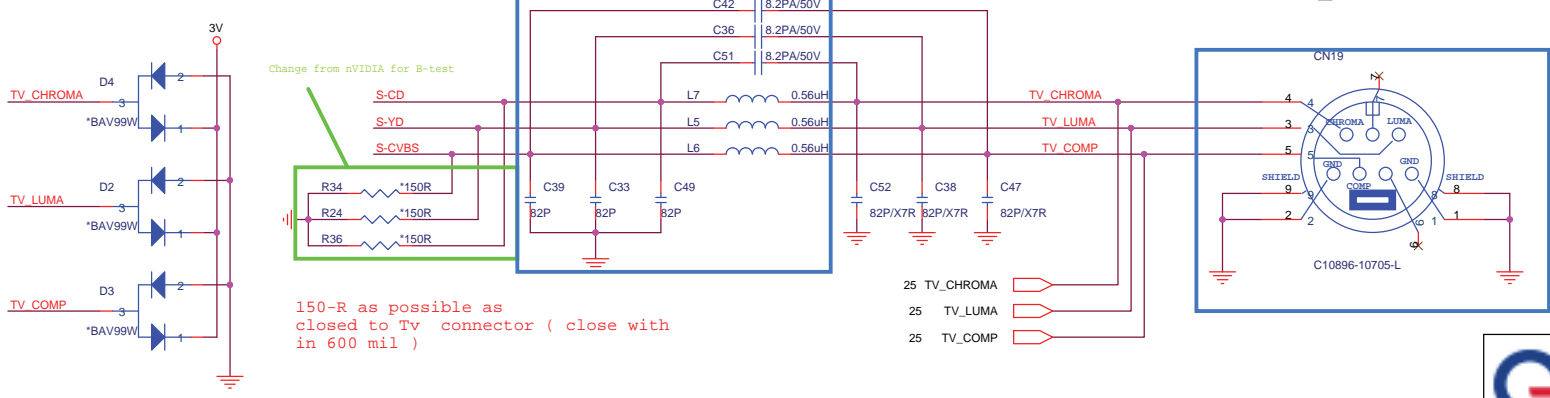


close within 600mils (close data switch)

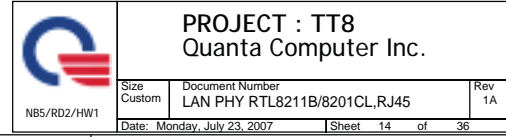
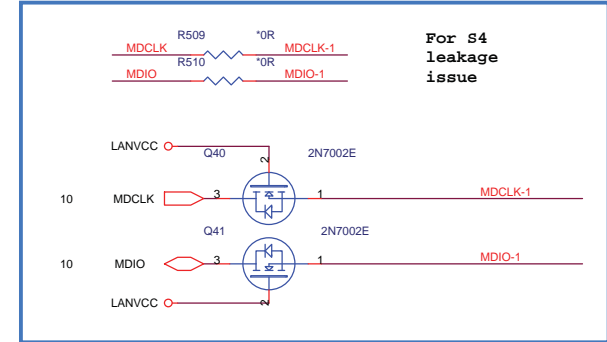


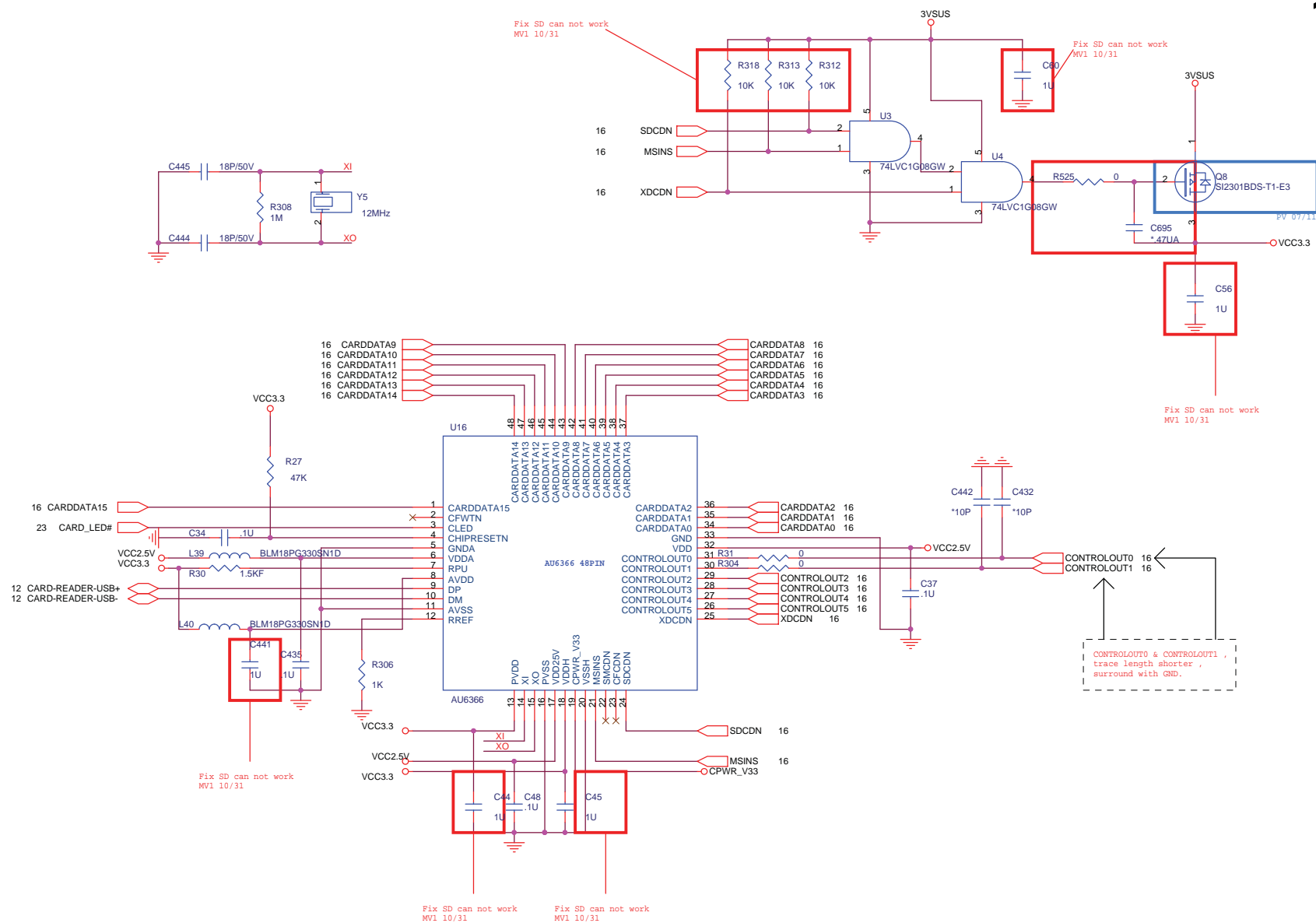
That is for CRT and TV choose.. used impedance and driver to choose

TV_OUT



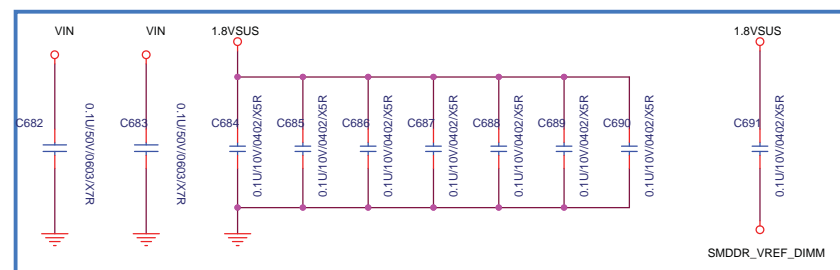
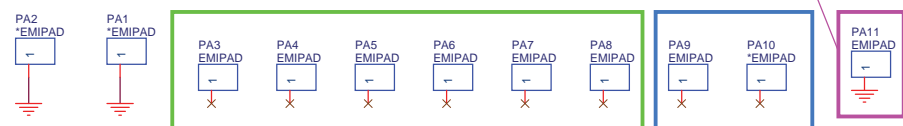
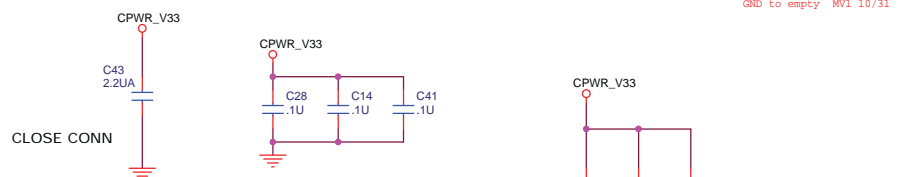
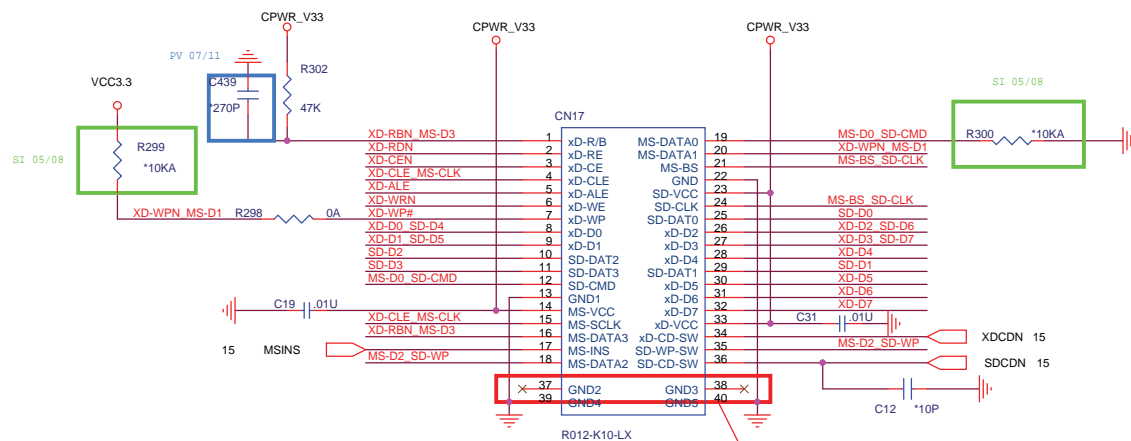
150-R as possible as closed to Tv connector (close with in 600 mil)





4 IN1 CARD READER

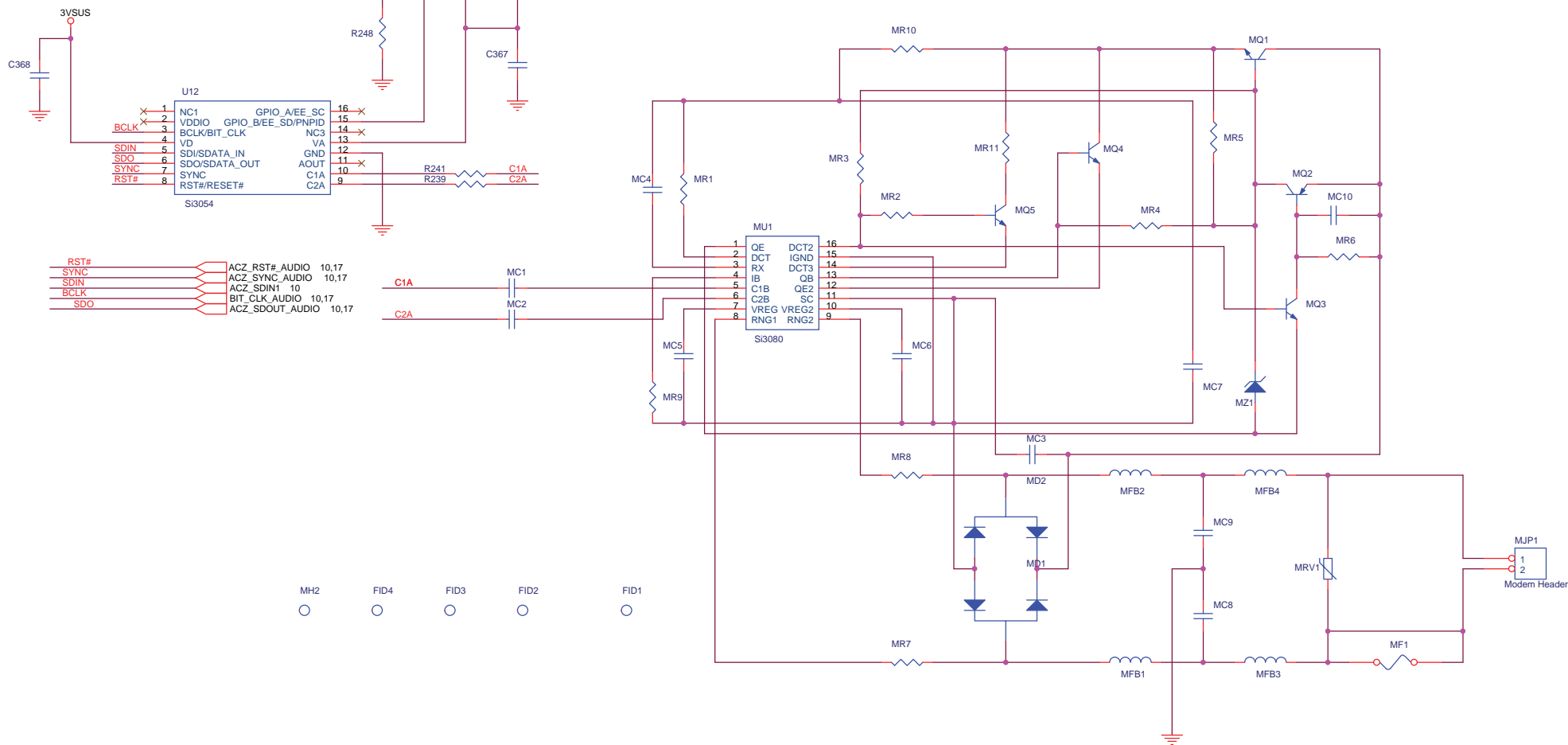
XD, MMC/SD, MS/MSP



PROJECT : TT8
Quanta Computer Inc.

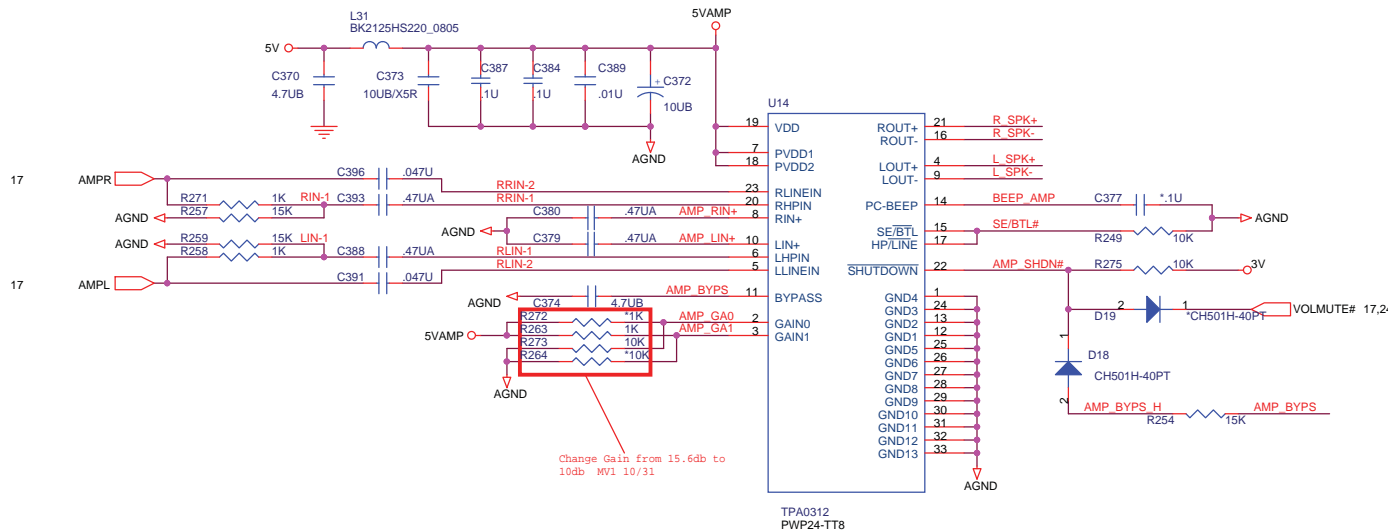
Size Custom	Document Number Card Reader	Rev 1A
Date: Monday, July 23, 2007	Sheet 16 of 36	





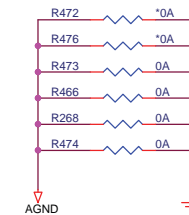
DESIGN SUBJECT TO CHANGE

SILICON LABORATORIES CONFIDENTIAL



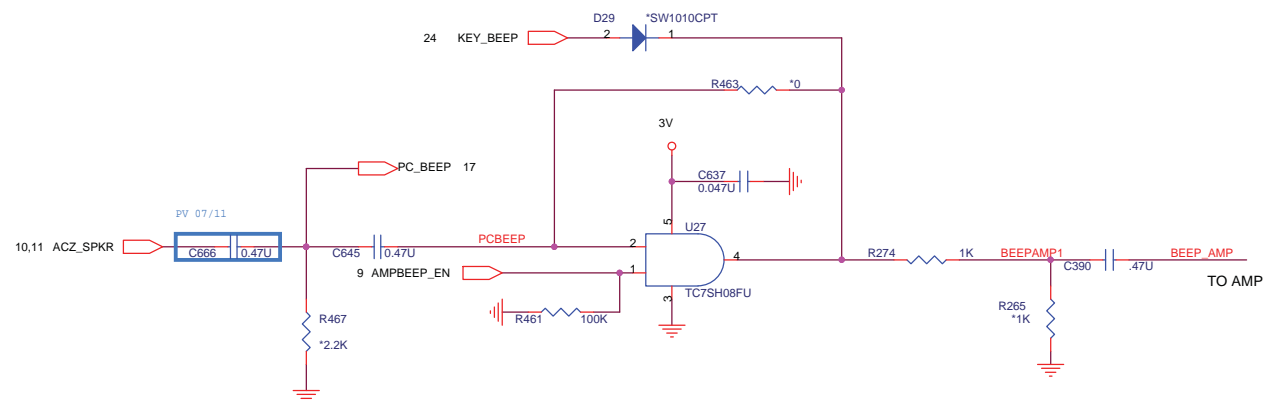
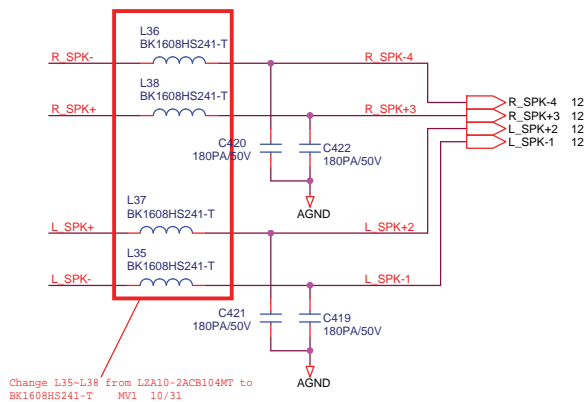
0312 Gain Table

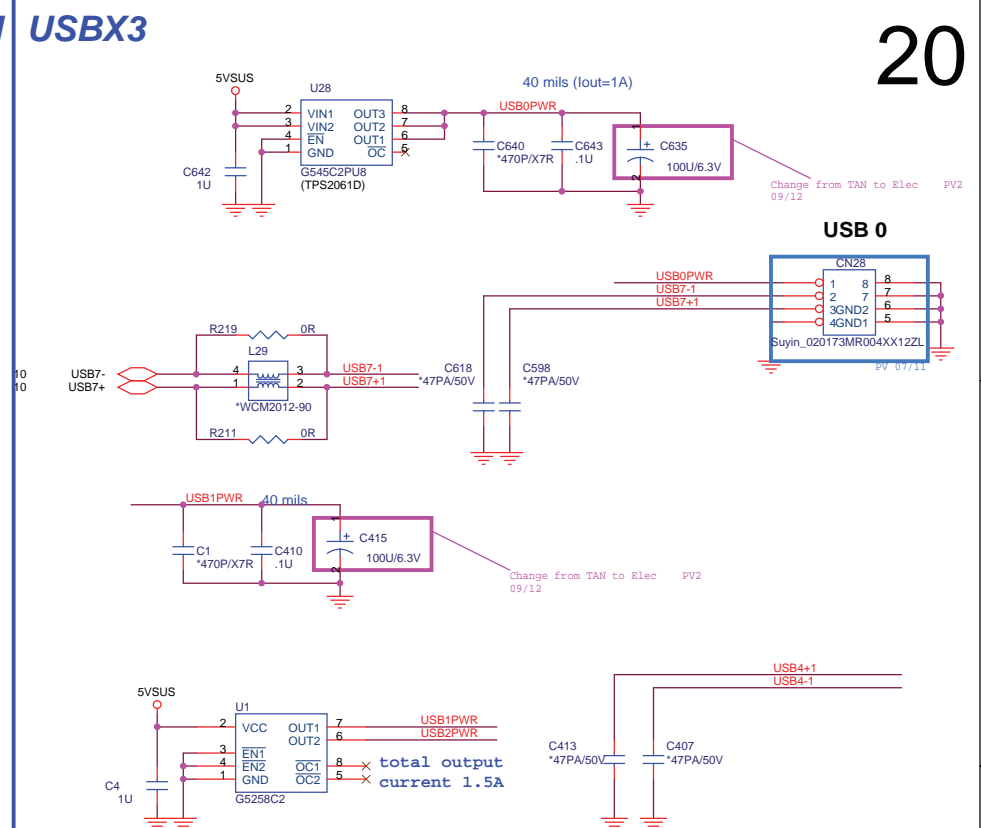
GAIN0	GAIN1	SE/BTL	AV(INV)
0	0	0	6dB
0	1	0	10dB
1	0	0	15.6dB
1	1	0	21.6dB
x	x	1	4.1dB



INT. SPEAKER

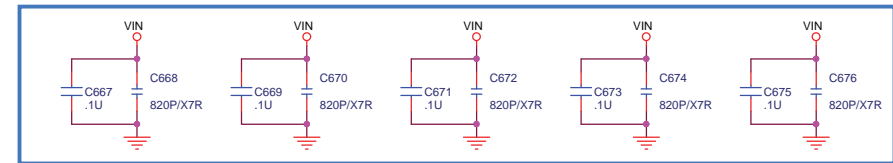
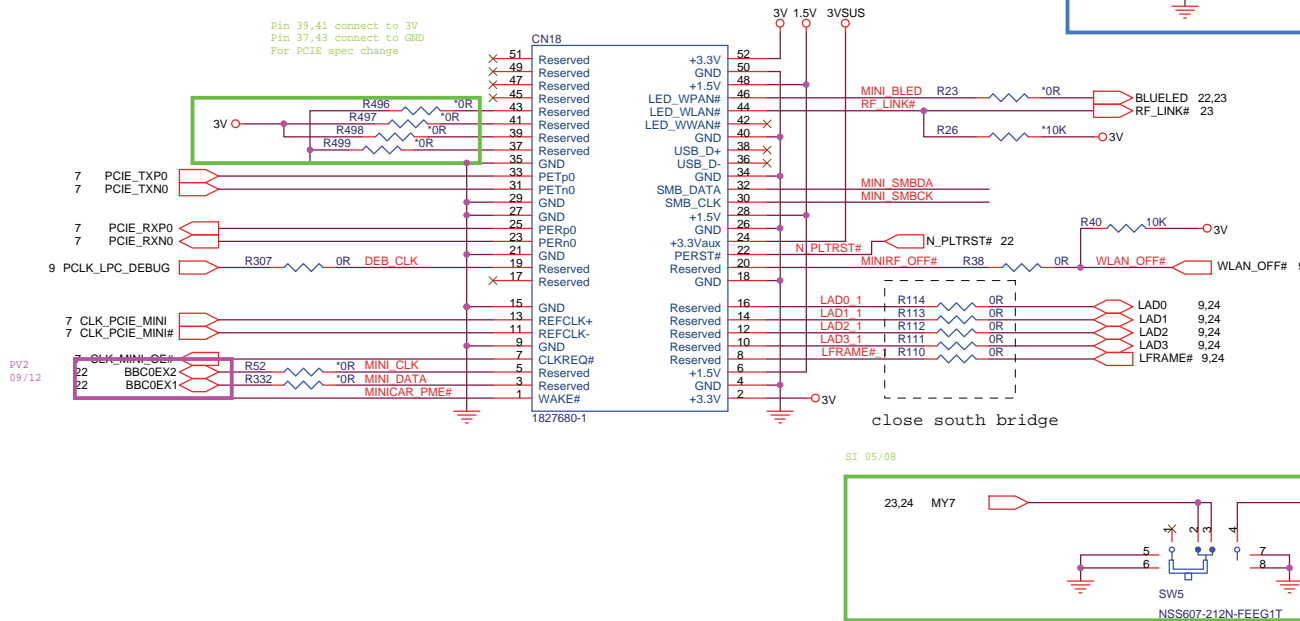
PCSPK BEEP





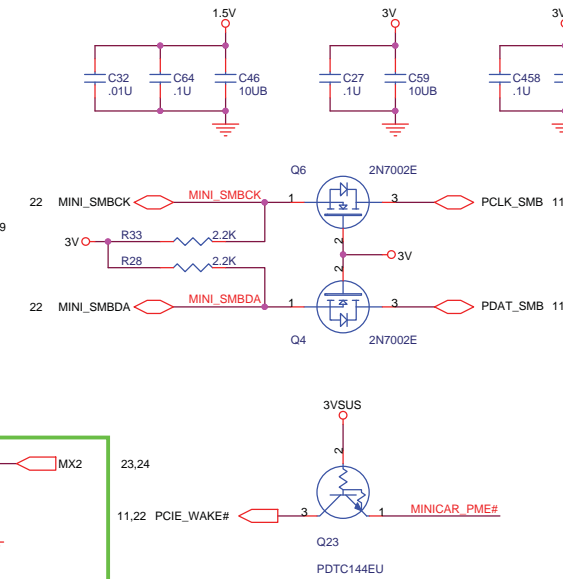
The schematic diagram illustrates the USB interface circuitry. It includes two WCM2012-90 connectors (L1 and L2) which are part of the USB3- and USB4- ports. These connectors are connected to the USB3+/- and USB4+/- signals. The circuit also features a CN10 connector with pins 1 through 8 labeled GND, 12, 11, 10, 9, 8, 7, and 6 respectively. Various passive components are shown, including resistors R1 through R4, capacitors C417 through C428, and a diode D419. A note indicates a change from TAN to Elec PV2 on 09/12.

Mini PCI-E Card 1 WLAN

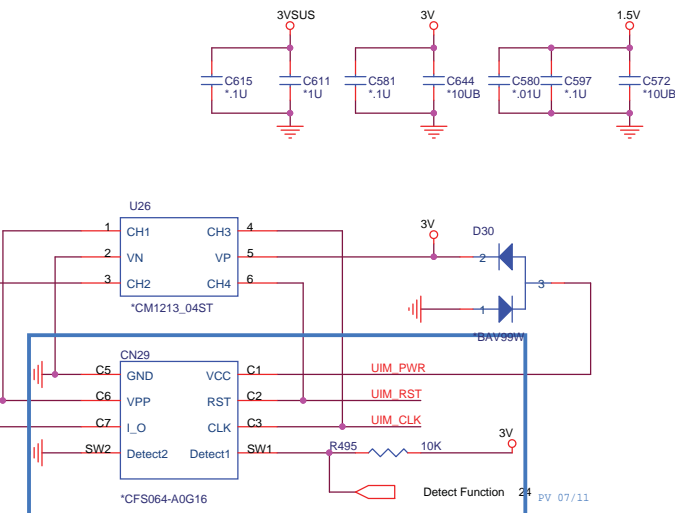
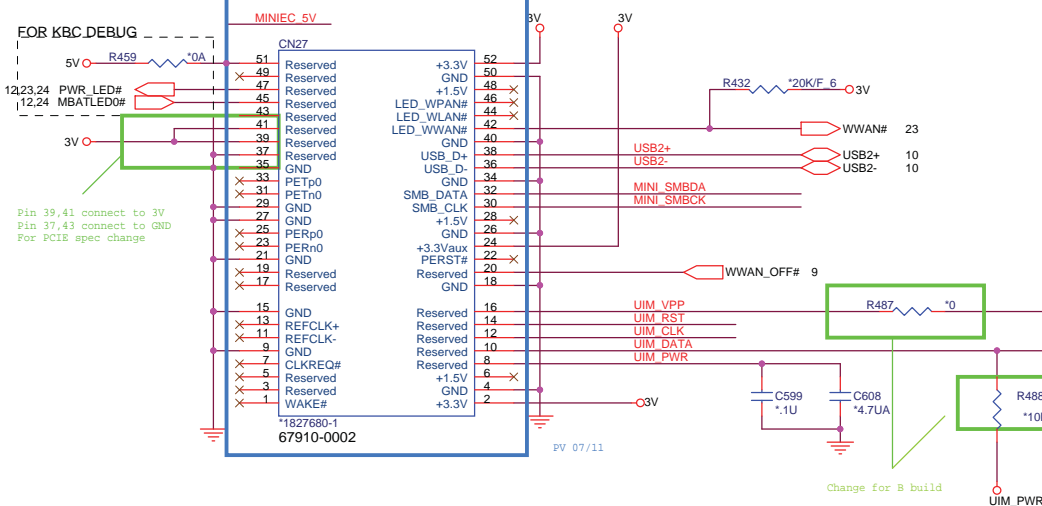


21

PV 07/11



Mini PCI-E Card 2 WWAN(W/SIM)



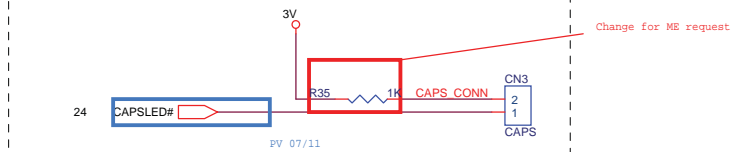
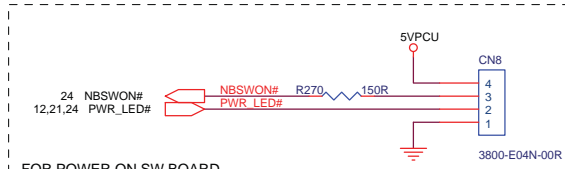
PROJECT : TT8
Quanta Computer Inc.

Size Custom	Document Number MINI CARD	Rev 1A
Date: Monday, July 23, 2007	Sheet 21 of 36	

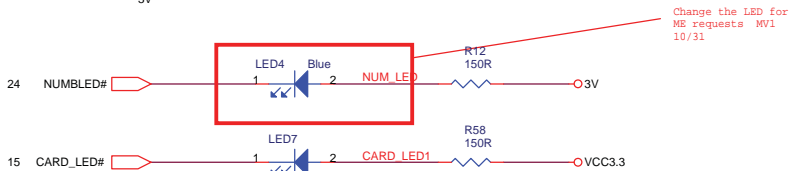
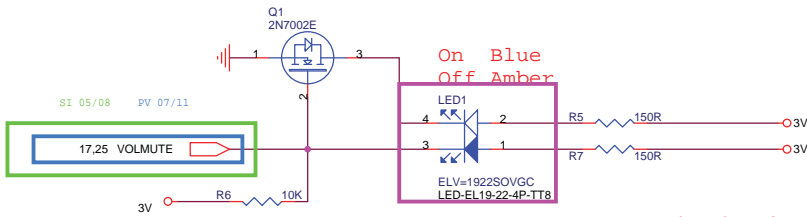
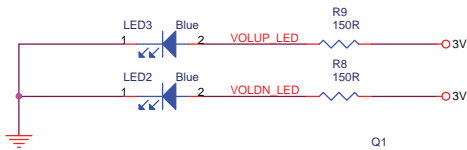


PROJECT : TT8
Quanta Computer Inc.

Size Custom	Document Number NEW CARD/BT	Rev 1A
Date: Monday, July 23, 2007		Sheet 22 of 36

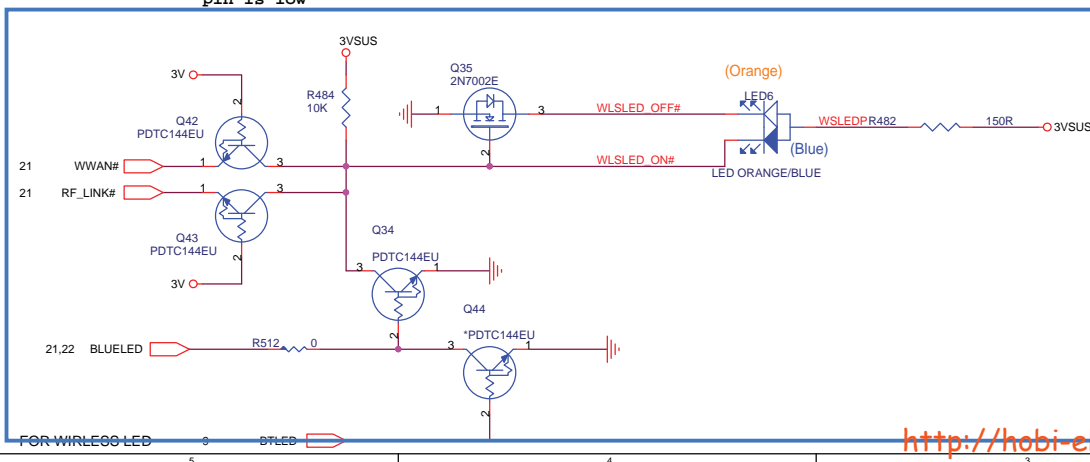


for caps lock LED board

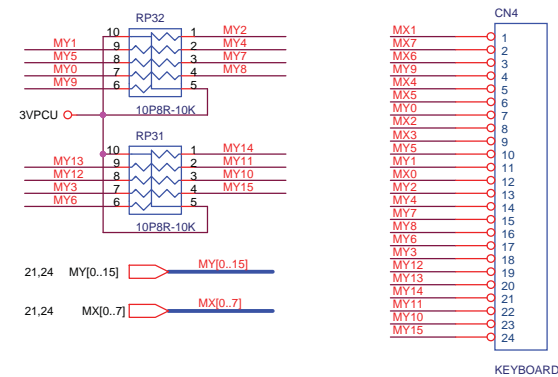


PV 07/11

insert card this
pin is low

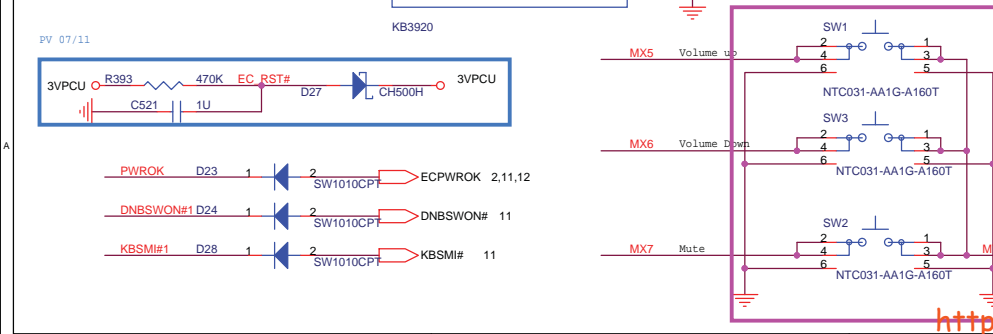
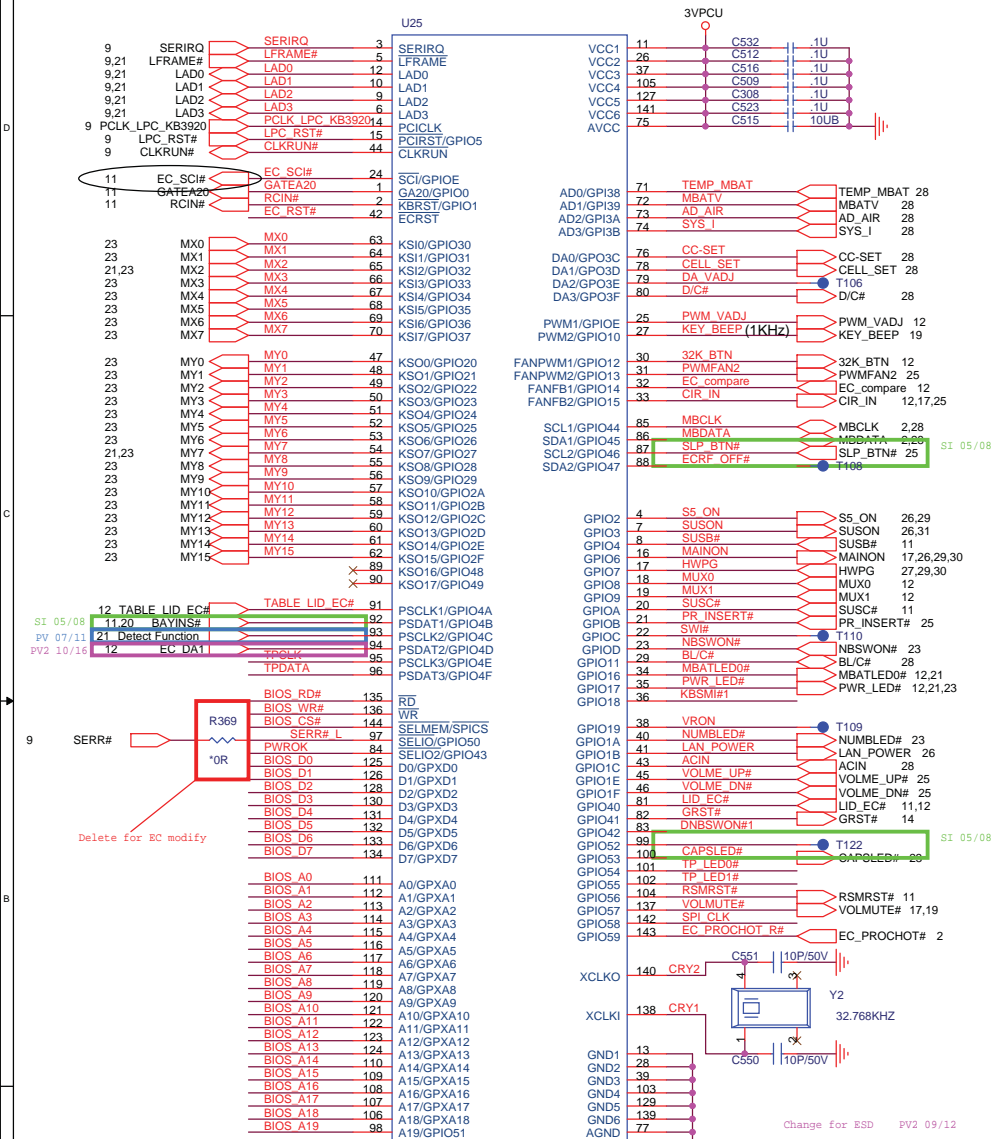
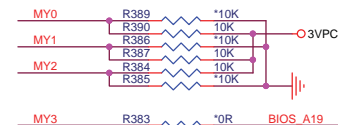


<http://hobi-elektronika.net>

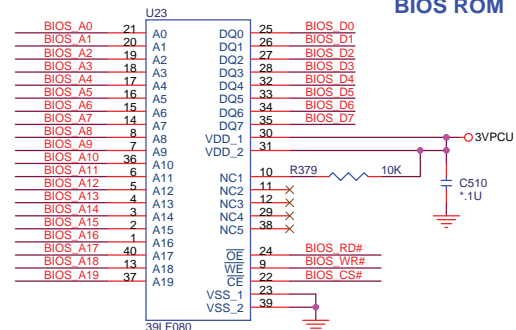


STRAP PIN

MY0	47	TP_TEST: Clock Test Mode Low: Test Mode HIGH: 32kHz clock in normal run
MY1	48	TP_PLL: PLL Test Mode Low: Test Mode HIGH: Normal operation
MY2	49	TP_SPI: Default flash access Low: Boot from SPI flash part HIGH: Boot from ISA flash part
MY3	50	TP_ISP: In-System Programming Mode Low: ISP mode HIGH: Normal Mode

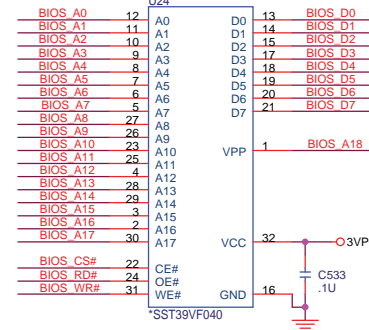


8Mbit (1M Byte), TSSOP40



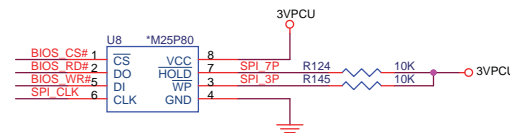
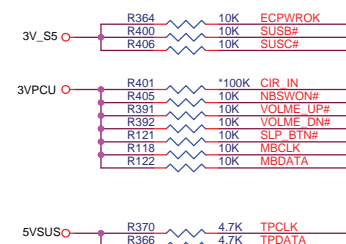
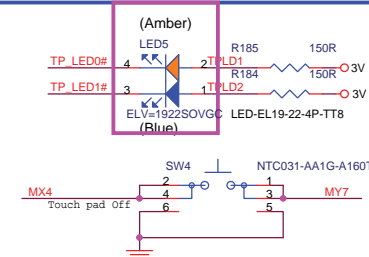
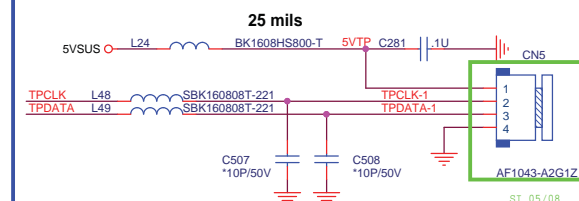
BIOS ROM

4Mbit (512k Byte), PLCC



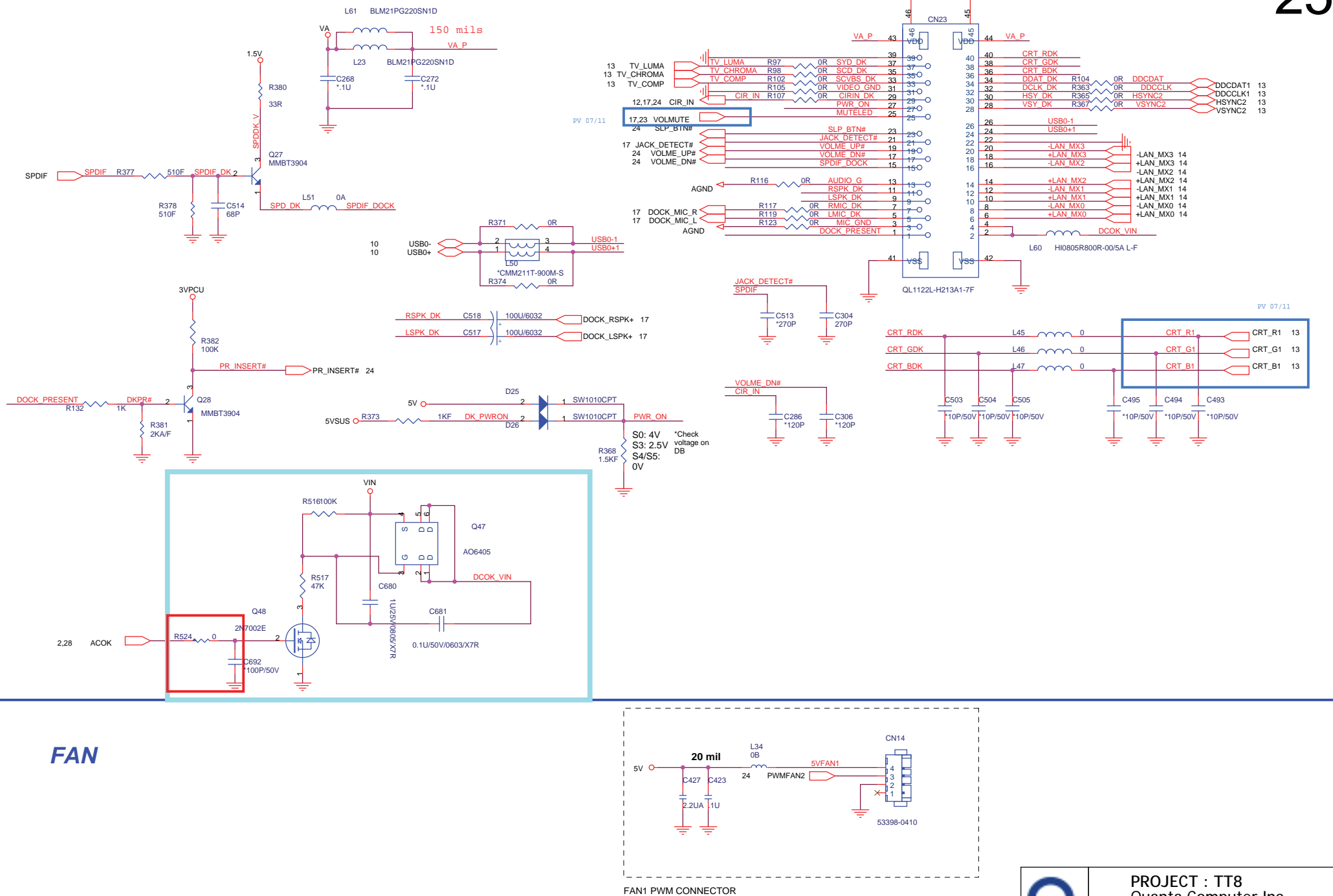
ROM CHIP P/N:AKE34ZAPK01

TOUCH PAD CONNECTOR



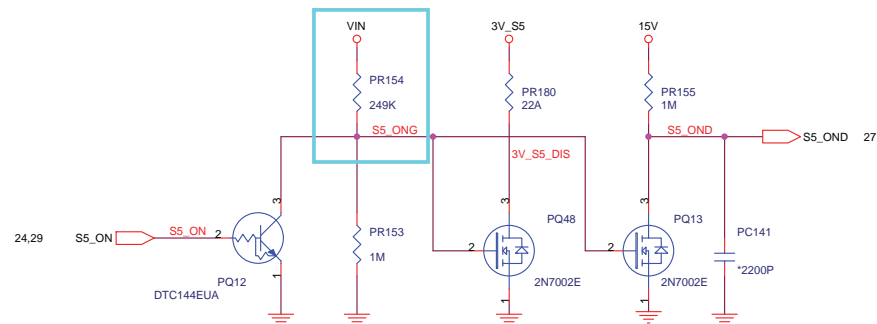
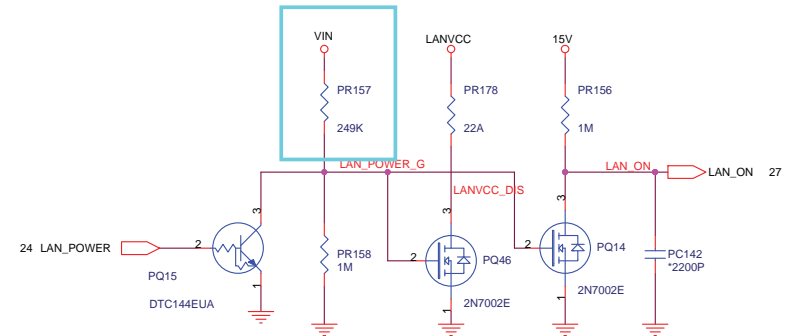
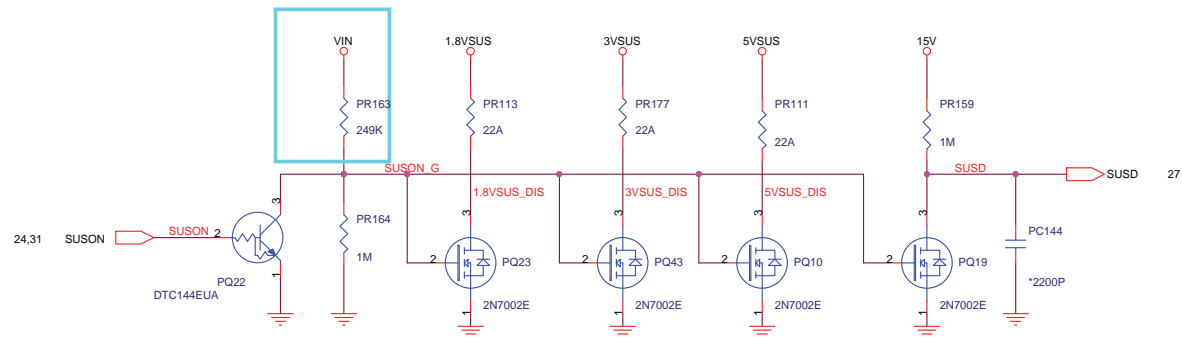
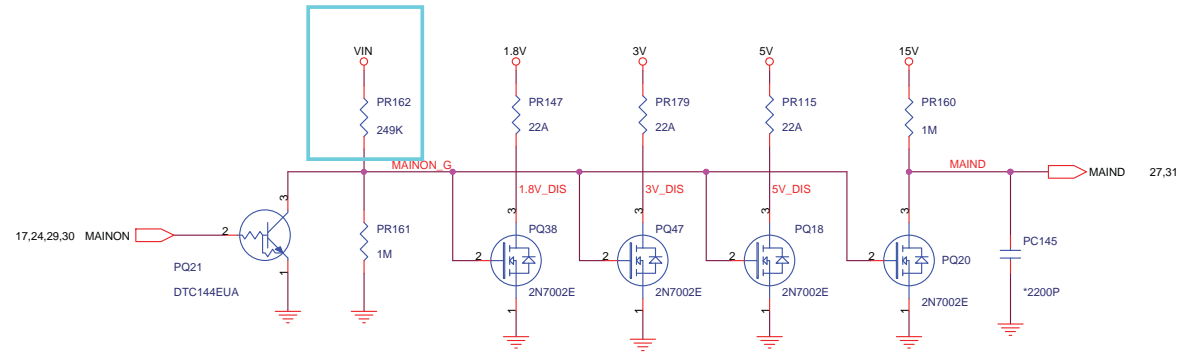
PROJECT : TT8
Quanta Computer Inc.

Size Custom	Document Number KB3920	R
Date: Monday, July 23, 2007		Sheet 24 of 36



FAN

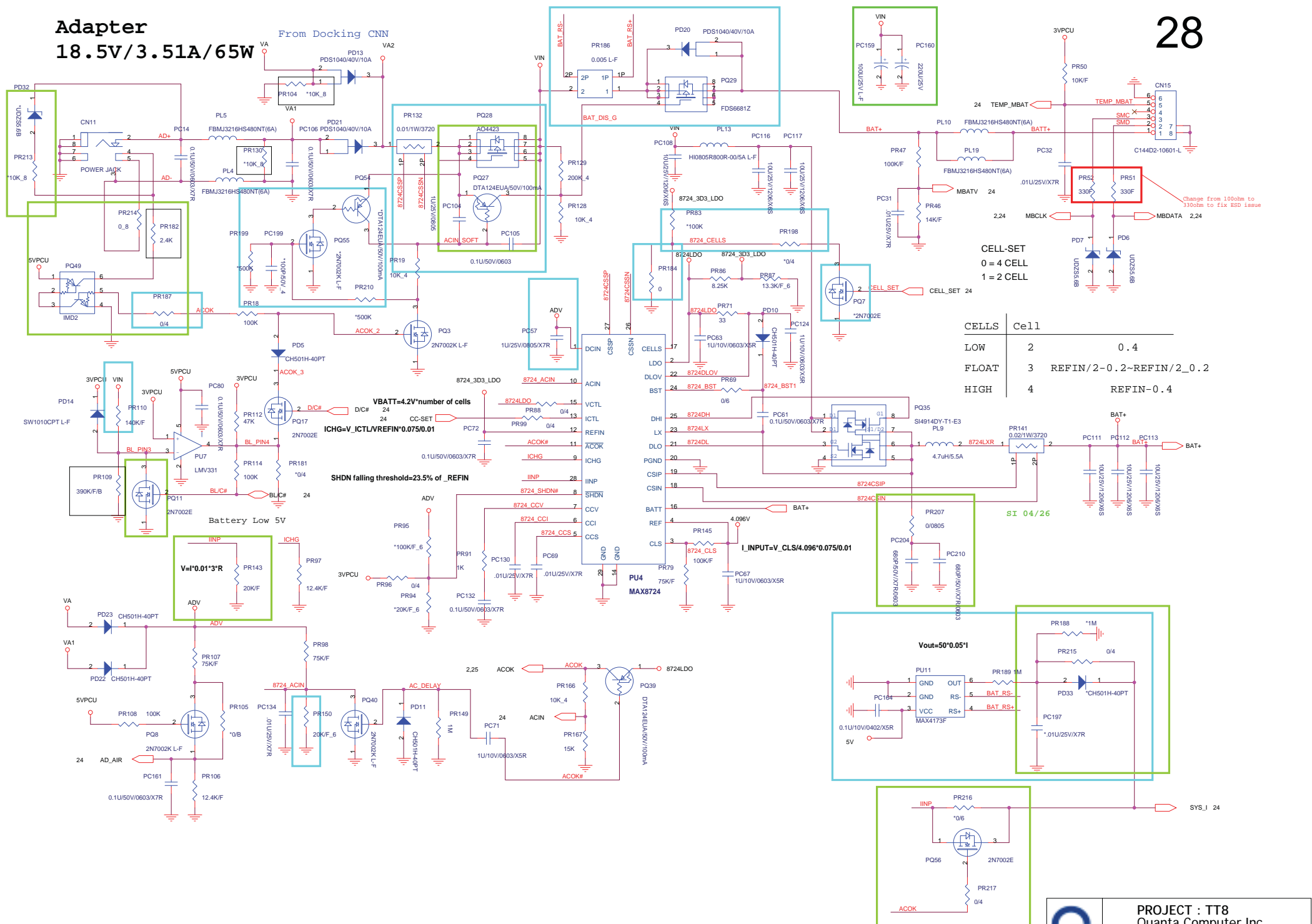
FAN1 PWM CONNECTOR

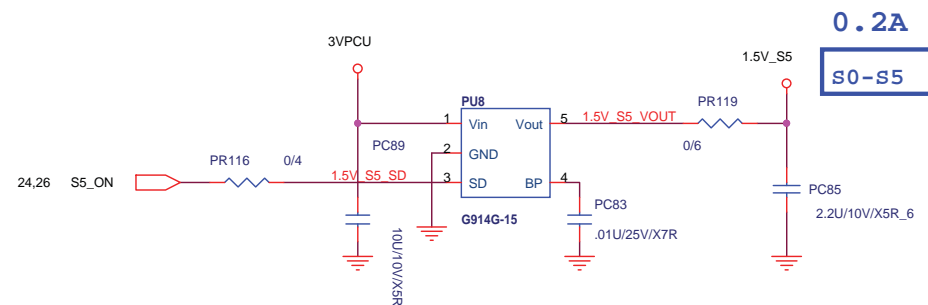
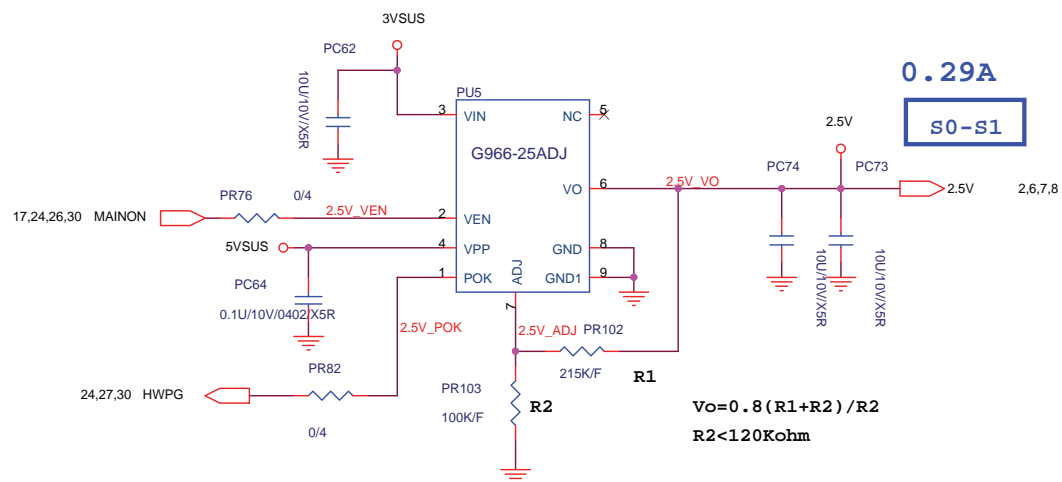


Adapter 18.5V/3.51A/65W

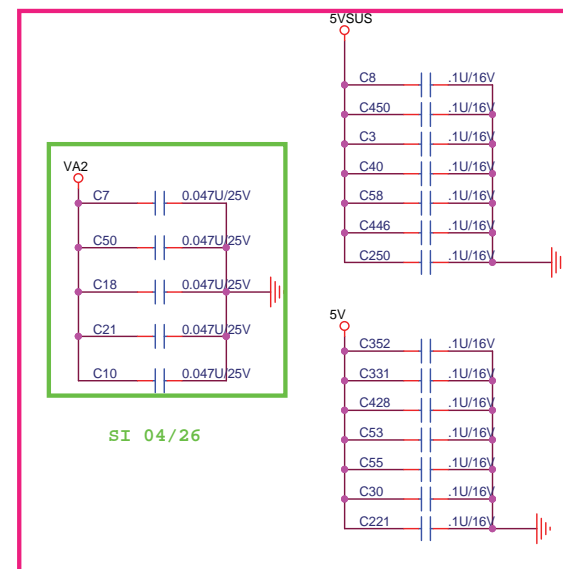
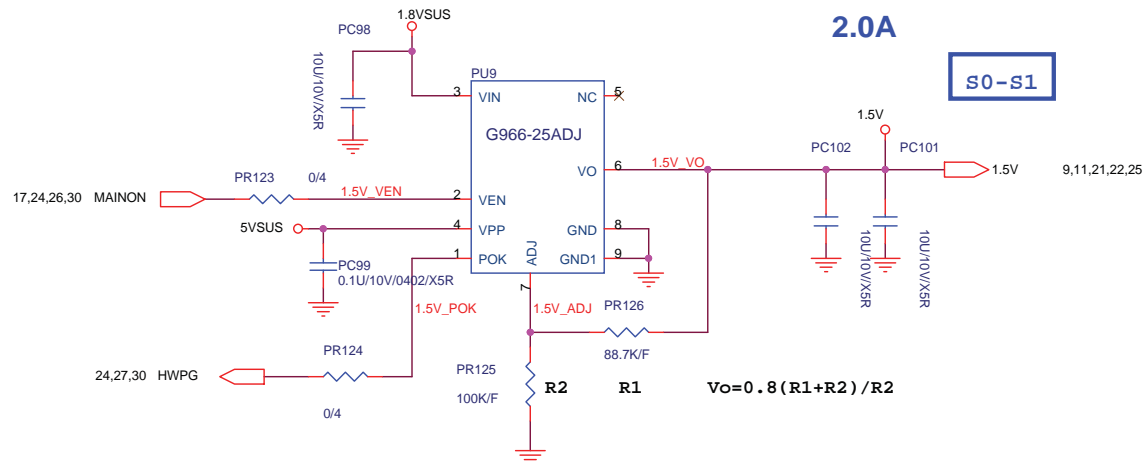
From Docking CNN

28





EMI



PROJECT : TT8
Quanta Computer Inc.

Size	Document Number	Rev
Custom	2.5V/1.5V_S5/1.5V	1A
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MAX1549

S0-S1

3A

$$V_{cs} = I_L(A) * L_DCR(m\Omega) = V_ILIM(mV) / 10$$

DCR 28m OHM

$$V_{out} = 0.5V(1 + R1/R2)$$

SI-2 modified

S0-S1

3.7A

$$V_{cs} = I_L(A) * L_DCR(m\Omega) = V_ILIM(mV) / 10$$

DCR 28m OHM

$$V_{out1} = 2.0V(REQ / (R_b + REQ))$$

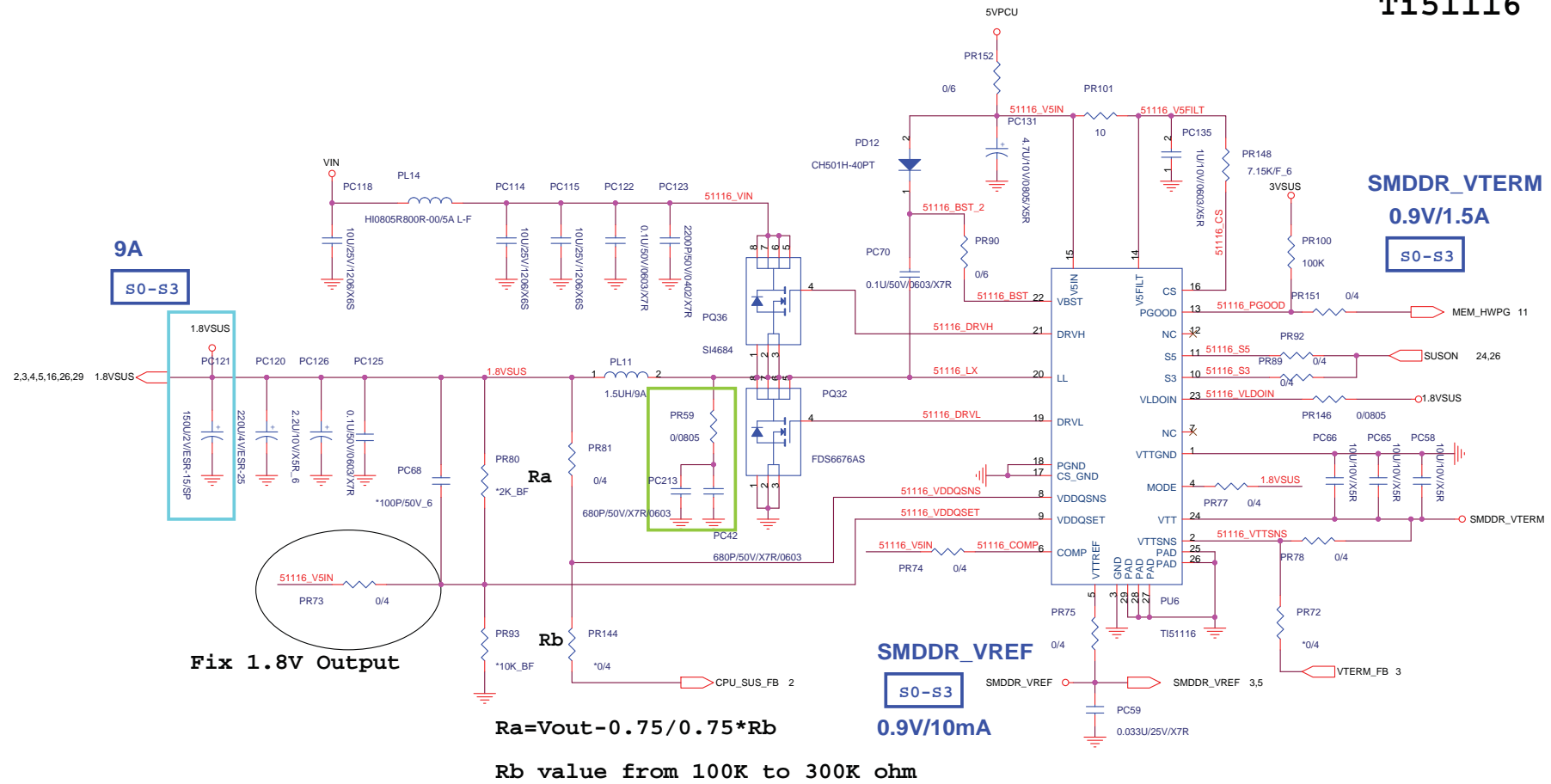
INPUTS		OUTPUTS			REQ	VOUT1
G1	G0	OD1	OD2	OD3		
0	0	High-Z	High-Z	Hight-Z	Ra=150K	1.2V
1	0	0	High-Z	Hight-Z	Ra//ROD1=100.1K	1.0V
0	1	High-Z	0	Hight-Z	Ra//ROD2=122.4K	1.1V
1	1	High-Z	High-Z	0	Ra//ROD3=82.02K	

FBLANK				
VCC	OPEN	REF	GND	
150us	100us	50us	blanking disabled	OU1 fault protection and PGO1 blanking
150us	100us	50us	100us	OU1 forced-PWM transition operation



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Quanta Computer Inc.

Size Custom	Document Number MAX1549 1.2V/1.2V_NB	Rev 1A
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Mode	Discharge Mode
V5IN	No discharge
VDDQ	Tracking discharge
Gnd	Non-tracking discharge

$$V_TRIP(mV) = R_TRIP(Kohm) * 10(uA)$$

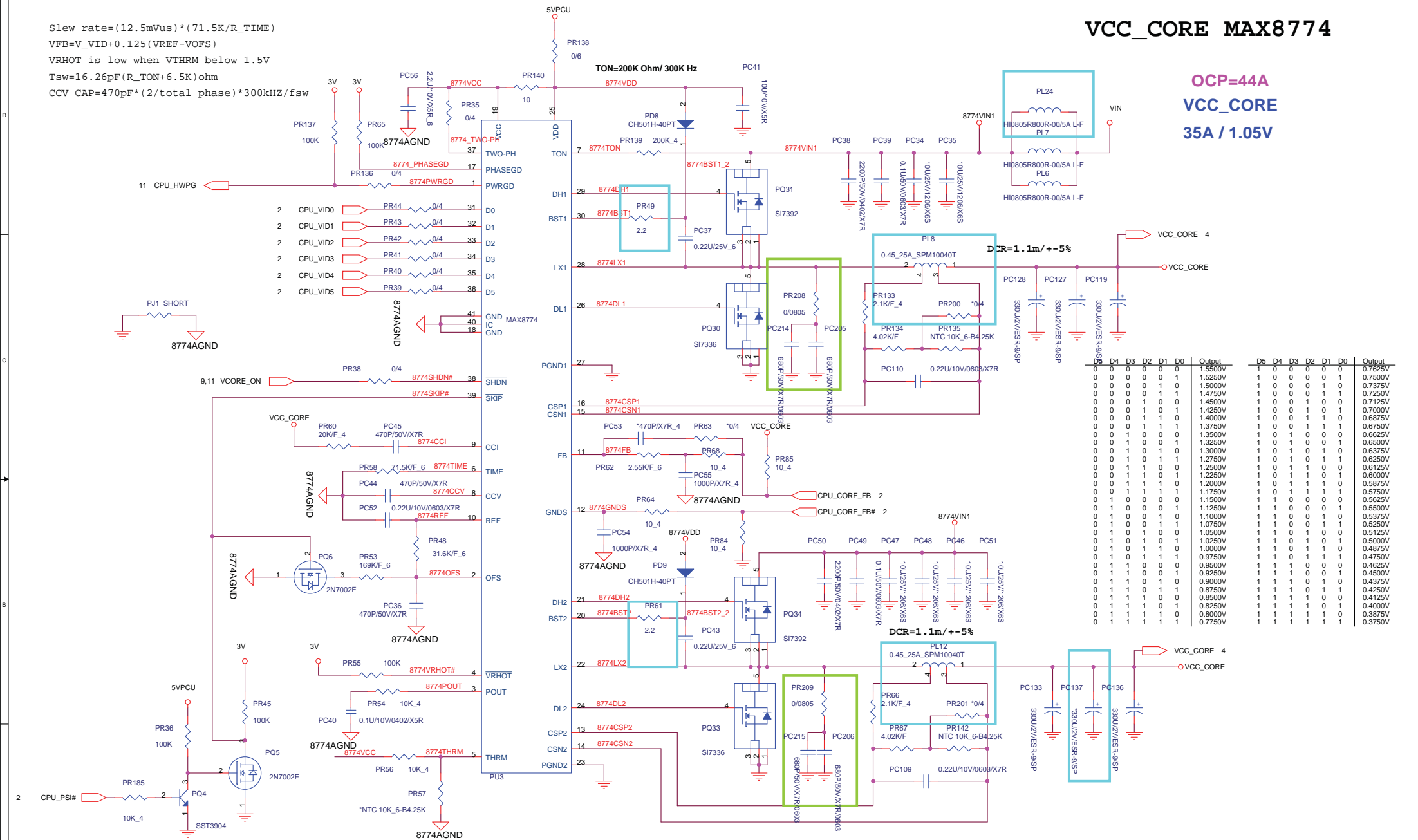
$$I_OCP = V_trip / Rds_on + I_Ripple / 2$$

VDDQSET	VDDQ(V)	VTTREF and Vtt	Note
GND	2.5	$V_vddqsns / 2$	DDR
V5IN	1.8	$V_vddqsns / 2$	DDR2
FB	adjustable	$V_VDDQSNS / 2$	$1.5V < VDDQ < 3V$

$Slew\ rate = (12.5mV\mu s) * (71.5K/R_TIME)$
 $VFB = V_VID + 0.125(VREF - VOFS)$
 VRHOT is low when VTHRM below 1.5V
 $Tsw = 16.26pF(R_TON + 6.5K)ohm$
 $CCV\ CAP = 470pF * (2 / total\ phase) * 300kHz / fsw$

VCC_CORE MAX8774

OCF=44A
VCC_CORE
35A / 1.05V




D5	D4	D3	D2	D1	D0	Output	D5	D4	D3	D2	D1	D0	Output
0	0	0	0	0	0	1.5500V	1	0	0	0	0	0	0.7625V
0	0	0	0	0	1	1.5000V	1	0	0	0	1	0	0.7375V
0	0	0	0	1	0	1.4750V	1	0	0	1	0	0	0.7250V
0	0	0	0	1	1	1.4500V	1	0	0	1	1	0	0.7125V
0	0	0	1	0	0	1.4250V	1	0	1	0	0	0	0.7000V
0	0	0	1	0	1	1.4000V	1	0	1	0	1	0	0.6875V
0	0	0	1	1	0	1.3750V	1	0	1	1	0	0	0.6750V
0	0	0	1	1	1	1.3500V	1	0	1	1	1	0	0.6625V
0	0	1	0	0	0	1.3250V	1	0	1	0	0	0	0.6500V
0	0	1	0	0	1	1.3000V	1	0	1	0	1	0	0.6375V
0	0	1	0	1	0	1.2750V	1	0	1	0	1	1	0.6250V
0	0	1	0	1	1	1.2500V	1	0	1	1	1	0	0.6125V
0	0	1	1	0	0	1.2250V	1	0	1	1	0	1	0.6000V
0	0	1	1	0	1	1.2000V	1	0	1	1	1	0	0.5875V
0	0	1	1	1	0	1.1750V	1	0	1	1	1	1	0.5750V
0	1	0	0	0	0	1.1500V	1	1	0	0	0	0	0.5625V
0	1	0	0	0	1	1.1250V	1	1	0	0	1	0	0.5500V
0	1	0	0	1	0	1.1000V	1	1	0	1	0	0	0.5375V
0	1	0	0	1	1	1.0750V	1	1	0	1	1	0	0.5250V
0	1	0	1	0	0	1.0500V	1	1	0	1	0	1	0.5125V
0	1	0	1	0	1	1.0250V	1	1	0	1	1	0	0.5000V
0	1	0	1	1	0	1.0000V	1	1	0	1	1	1	0.4875V
0	1	0	1	1	1	0.9750V	1	1	0	1	1	1	0.4750V
0	1	1	0	0	0	0.9500V	1	1	1	0	0	0	0.4625V
0	1	1	0	0	1	0.9250V	1	1	1	0	1	0	0.4500V
0	1	1	0	1	0	0.9000V	1	1	1	0	1	1	0.4375V
0	1	1	0	1	1	0.8750V	1	1	1	1	0	0	0.4250V
0	1	1	1	0	0	0.8500V	1	1	1	1	0	1	0.4125V
0	1	1	1	0	1	0.8250V	1	1	1	1	1	0	0.4000V
0	1	1	1	1	0	0.8000V	1	1	1	1	1	1	0.3875V
0	1	1	1	1	1	0.7750V	1	1	1	1	1	1	0.3750V

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Quanta Computer Inc.

Size Custom	Document Number MAX8774 VCC_CORE	Rev 1A
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MODEL	DB1 --->SI1	CHANGE LIST	Model	OT1 MB BOARD	
			Page	FROM	TO
TT8 MB 31TT8MB0006	4/17-4/20	1.Change Audio port and senser pin resistor. Internal MIC change from Pin14,15 to Pin16,17 Docking Mic Change from Pin16,17 to Pin14,15 Docking spk change from Pin23,24 to Pin 43,44 Swap Pin30 and Pin31 Change R486 from Pin 13 to Pin 34 and change from 5.1KK to 10K Change R251 10K to R485 5.1K 2.Change WWAN and WLAN Pin define Add R487 and R488 3.Change TEMP Control chip for leakage, Change Q9 and Q10 to BAM70020074 4.Change HDD connector type, RJ45/CRT connector footprint 5.Swap LCD connector singnal from machine require 6.Swap U5 CRT/TV singnal from nVIDIA require 7.Change battery and D30 footprint 8.Change C251,C242,C138,C66,C71,C276,C277 footprint from 0603 to 0402 9.Add Q36,Q37,R489,C661,R490 for Docking MIC detect 10.Change SW5 and CN8 footprint for machinecal request 11.Change L41 to PBY201209T-300Y-N (Footprint : 0805) 12.Delect H3 and H4 for machinecal change 13.Change C20 from 0.1U to 1U (Fix LCD rise time) 14.Move Net "SLP_BTN# from pin99 to pin87 15.Modify Docking mute LED circuit 16.Modify U25 SCI# signal from BIOS request, AddR491,R492 17.Modify Buletooth switch and ODD BAYINS# to EC 18.Change caps lock connector footprint from machencal request 19.Add U30,R495,R494,R493,Q38 for reserve SIM card 20.Change 4-in-1 card footprint 21.Add R44,R43,R48 Remove R62,R64,R69,R34,R24,R36 22.Change L45,L46,L47 to 0 ohm Del C503,C504,C505,C493,C494,C495 for D-SUB function	1	1A	
			2	1A	
			3	1A	
			4	1A	
			5	1A	
			6	1A	
			7	1A	
			8	1A	
			9	1A	
			10	1A	
			11	1A	
			12	1A	
			13	1A	
			14	1A	
			15	1A	
			16	1A	
			17	1A	
			18	1A	
			19	1A	
			20	1A	
			21	1A	
			22	1A	
			23	1A	
			24	1A	
			25	1A	
			26	1A	
			27	1A	
			28	1A	
			29	1A	
			30	1A	
			31	1A	
			32	1A	
			33	1A	




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Quanta Computer Inc.

Size Custom Document Number --> SI** Change history Rev 1A

Date: Monday, July 23, 2007 Sheet 33 of 36

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MODEL		CHANGE LIST	Model	OT1 MB BOARD	
SI1 --->PV1	Page		FROM	TO	
TT8 MB 31TT8MB0006	5/17~7/11	1.Exchange Audio port External MIC Exchange Pin22 and Pin21 CD Line Exchange Pin18 and Pin20 Internal MIC Exchange Pin16 and Pin17 Docking Mic Exchange Pin14 and Pin15 3.Change R478 from 22ohm to 0ohm 4.Change R462 0ohm to C666 0.47u for Audio chip distortion 5.Exchange R272 and R263, R273 and R264 for amplifier gain change 6.Change Q8 from BAM51030Z15 to BAM23010Z30 for Rdson issue 7.Remove C439 for MS pro card can not detect 8.Add C667,C668,C669,C670,C671,C672,C673,C674,C675,C676 for WLAN con not detect issue 9.Add reverse circuit for LED issue 10.Delect Q7 for Cap lock LED 11.Add EMI Cap C93,C118,C496,C497,C499,C566,C589,C555,C334,C337 12.Change CN19,CN27,CN28,CN29 footprint 14.Change Sim connector (Add detect pin) 15.Move Docking CRT signal after PI circuit 16.Add R500, R501 for Audio chip function 17.Add D37 and R502 for nVIDIA solution 18.Move D22 from +5VCRT to +5VCRT3 19.Change Docking detect circuit 20.Delet H20 H21 21.Exchange MINI_DATA and MINI_CLK 22.Add Diode for SATA and ODD LED control 23.Add power controller for 5V shutdown 24.Change WLAN LED circuit 25.Add Res for ACZ signal 26.Delete H7 and H14 for ME change 27.Modify SB to Audio and Modem signal	1	1A	
			2	1A	
			3	1A	
			4	1A	
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			6	1A	
			7	1A	
			8	1A	
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			10	1A	
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			33	1A	



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MODEL		CHANGE LIST		Model	OT1 MB BOARD	
				Page	FROM	TO
TT8 MB 31TT8MB0006	PV1 --->PV2 9/8-10/17	1.Page17 change voltage from +3V to 3V fix the Mic can not work 2.Page17 change R14 from 4.7K to 5.6K to fix LCCVDD rise time 3.Page17 change LCD cable Pin22 and Pin15 for switch function, Pin7 change to 32K_BTN 4.Page24 add GPIO for switch function 5.Page10 Change cap from 18p to 22p 6.Page17 Change C392 and C395 from 10U to 1U to fix Docking noise 7.Page16 add PA11(EMI spring) 8.Page21 Exchange BBC0EX1 and BBC0EX2 9.Page20 remove C614, C607, C406, C414, C404, C405 10.Page20 Change C635, C415, C416 from TAN to ELEC 11.Page11 Del R205 and Add R207 for Bios check		1	1A	
				2	1A	
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				32	1A	
				33	1A	


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MODEL		CHANGE LIST		Model	OT1 MB BOARD	
				Page	FROM	TO
TT8 MB 31TT8MB0006	PV2 --->MV1 10/17-11/15	<p>1.Page10 Exchange USB0+/- with USB3+/- signal</p> <p>2.Page12 Change CN12 Pin1 from 5VSUS to 3V</p> <p>3.Page17 Change C648 and C656 from 4.7U to 22U to fix Vista issue</p> <p>4.Page19 Change L35-L38 from LZA10-2ACB104MT to BK1608HS241-T</p> <p>5.Page19 Change Gain from 15.6db to 10db</p> <p>6.Page17 Del R260,R267,D312,D322 for Docking MIC</p> <p>7.Page17 ADD R520,R521,R522,R523 for Docking MIC</p> <p>8.Page21 Change PR51 PR52 from 100ohm to 330ohm to fix ESD issue</p> <p>9.Page20 unstuff R188 to fix ODD problem</p> <p>10.Page11 Change the board ID1 from low to high</p> <p>11.Page15 Change Cap (C60,C56,C441,C44,C45)from 0.1u to 1u</p> <p>12.Page15 Change Res (R318,R313,R312)from 39K to 10K</p> <p>13.Page17 Add 0.01u(C693, C694) to fix high frequency problem</p> <p>14.Page14 remove the cap(C408,C409) from MV build</p> <p>15.Page7 Reserve C696 for nVIDIA</p> <p>16.Page15 Reserve R525 and C695 for 3VSUS drop</p> <p>17.Page23 Change LED4 for ME requests</p>		1	1A	
				2	1A	
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